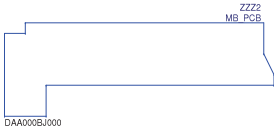


MODEL NAME : Celtic
PCB NO : LA-D312P
BOM P/N :



	R1	R3	R3	R3	R3
CPN	DAA000BJ000	DAA000BJ000	DAA000BJ000	DAA000BJ000	DAA000BJ000

Dell/Compal Confidential

Schematic Document

Celtic (Skylake Y)

2015-12-10
Rev: 1.0

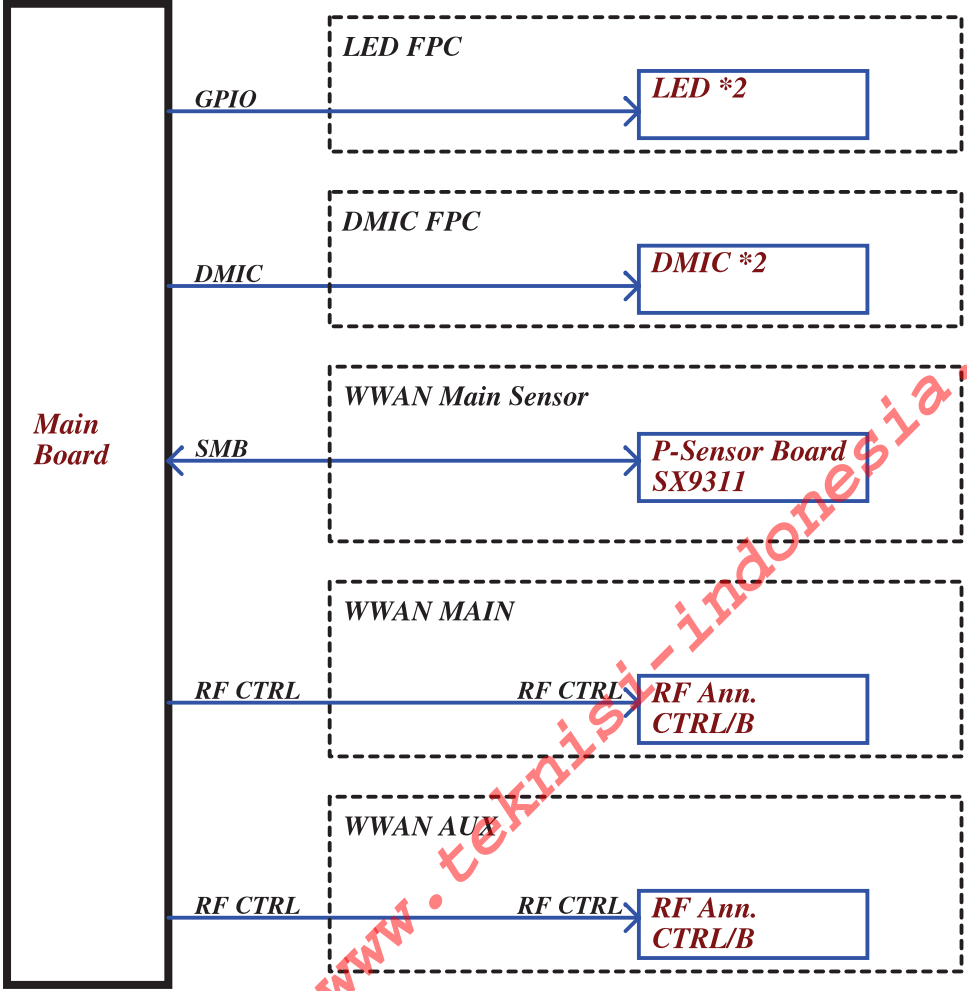
AR Option



CPU Option



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				Date	Friday, December 25, 2015
				Sheet	1 of 61
				Rev	0.3



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					DaughterB block diagram
					Size Document Number
					LA-D311P
					Rev 0.3
					Date: Friday, December 25, 2015
					Sheet 3 of 51

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ Power plane	+3VALW_DSW +3VALW +1.8VALW +3VLP	+3V_PRIM +1.8V_PRIM +1.0V_PRIM +1.0VA_GATE +0.95V_PRIM	+1.2V_DDR +3.3V_CV2 +1.8V_MEM +1.0V_VCCST	+5VS +3VS +1.8VS +1.0V_VCCSTG +0.85VS_VCCIO +0.6VS_VTT +VCC_SA +VCC_GT +VCC_CORE
S0	ON	ON	ON	ON
S3 /AC	ON	ON	ON	OFF
DS3	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	BATT	Charger	XDP	USH	PD Controller -1	PD Controller -2	GPIO Expander	P-sensor
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH								
MEM_SMBCLK MEM_SMBDATA	PCH			V					
EC_SMB00_CLK EC_SMB00_DAT	MEC1641								
EC_SMB01_CLK EC_SMB01_DAT	MEC1641				V				V
EC_SMB03_CLK EC_SMB03_DAT	MEC1641	V							
EC_SMB04_CLK EC_SMB04_DAT	MEC1641		V						
EC_SMB05_CLK EC_SMB05_DAT	MEC1641					V			
EC_SMB07_CLK EC_SMB07_DAT	MEC1641						V		

Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	PCB Revision	REV
0	240K +/- 5%	4700p	0.1	EVT1.0
1	130K +/- 5%	4700p	0.2	DVT1.0/DVT1.1
2	62K +/- 5%	4700p	0.3	DVT2.0/PreMP
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	NC			

SOC DDI Port Mapping	DDI PORT#	DESTINATION
	B	Alpine Ridge
	C	DP MUX

SOC PCIE Port Mapping	PCI EXPRESS	DESTINATION
	Lane 1	Alpine Ridge
	Lane 2	
	Lane 3	
	Lane 4	
	Lane 5	NGFF (WLAN)
	Lane 6	NGFF (WiGig)
	Lane 7	NGFF (SSD)
	Lane 8/ SATA 1	
	Lane 9	Cardreader
	Lane 10	HCA

Lane reversal

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE1	TBT
	CLKOUT_PCIE2	NGFF (WiGig) or (HCA)
	CLKOUT_PCIE3	Cardreader
	CLKOUT_PCIE4	NGFF (SSD)
	CLKOUT_PCIE5	NGFF (WLAN)

USB 3.0 PORT#	DESTINATION
1	Type A(Debug)
2	WWAN
3	
4	

USB 2.0 PORT#	DESTINATION
1	Type A(Debug)
5	WWAN
7	USH
3	Touch
9	CAM
2	BT

FLEX CLOCKS	DESTINATION
CLKOUT_LPC_0	EC LPC
CLKOUT_LPC_1	Debug

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	sm	0.50000
1	Top		Copper foil	0.33oz+plating	1.20000
			Prepreg	1086	2.65000
2	IN1(GND)		Copper foil	0.33oz+plating	1.10000
			Prepreg	106	1.80000
3	GND/PWR		Copper foil	0.33oz+plating	1.10000
			Prepreg	1080	2.56000
4	IN2		Copper foil	0.5oz	0.60000
			Core	3mil	3.00000
5	GND/PWR		Copper foil	0.5oz	0.60000
			Prepreg	106	1.63000
6	GND/PWR		Copper foil	0.5oz	0.60000
			Core	3mil	3.00000
7	IN3		Copper foil	0.5oz	0.60000
			Prepreg	1080	2.56000
8	GND/PWR		Copper foil	0.33oz+plating	1.10000
			Prepreg	106	1.80000
9	IN4(GND)		Copper foil	0.33oz+plating	1.10000
			Prepreg	1086	2.65000
10	Bottom		Copper foil	0.33oz+plating	1.20000
			SolderMask	sm	0.50000
Overall Thickness (0.8mm ± 10%)					31.85000
					0.80899

Symbol Note :

@ : means de-pop

⬇ : means Digital Ground

⬇ : means Analog Ground

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						Size		Document Number		Rev	
								<i>LA-D311P</i>		0.3	
						Date:		Friday, December 25, 2015		Sheet 4 of 61	

Functional Strap Definitions

GPP_E19 (Internal Pull Down): DDPB_CTRLDATA

0 = Port B is not detected.

1 = Port B is detected.

GPP_E21 (Internal Pull Down): DDPC_CTRLDATA

0 = Port C is not detected.

1 = Port C is detected.

GPP_E23 (Internal Pull Down): DDPD_CTRLDATA

0 = Port D is not detected.

1 = Port D is detected.

PU/PD for CPU JTAG signals

+1.0V_VCCST
RC95 1 2 1K 0402 1% H_THERMTRIP#

+3V_PRIM
RH1481 2 10K 0201 5% SIO_EXT_SMI#

+1.0V_XDP
RC2781 XDR@ 2 100K 0201 5% XDP_PSENT#

+1.0V_VCCSTG
RC19 2 1 51 0402 5% XDP_PREQ#

RC20 2 1 51 0402 5% CPU_XDP_TCK

RC25 2 1 51 0402 5% CPU_XDP_TDI

RC18 2 1 51 0402 5% CPU_XDP_TDO

RC40 1 2 2 1K 0402 5% XDP_ITP_PMODE

RC23 2 1 51 0402 5% CPU_XDP_TCK

RC24 2 1 51 0402 5% CPU_XDP_TRST#

CC161 1 2 1 0.1u 0201 10V6K XDP@

CC162 1 2 1 0.1u 0201 10V6K XDP@

RC37 2 1 51 0402 5% PCH_JTAG_TMS

RC34 2 1 51 0402 5% PCH_JTAG_TDI

RC38 2 1 51 0402 5% PCH_JTAG_TDO

RC41 2 1 51 0402 5% PCH_JTAGX

RC35 2 1 51 0402 5% PCH_JTAG_TCK

RC36 2 1 51 0402 5% PCH_JTAG_TMS

RC39 2 1 51 0402 5% PCH_JTAG_TDI

RC42 2 1 51 0402 5% PCH_JTAG_TDO

RC45 2 1 51 0402 5% PCH_JTAGX

RC48 2 1 51 0402 5% PCH_JTAG_TCK

RC51 2 1 51 0402 5% PCH_JTAG_TMS

RC54 2 1 51 0402 5% PCH_JTAG_TDI

RC57 2 1 51 0402 5% PCH_JTAG_TDO

RC60 2 1 51 0402 5% PCH_JTAGX

RC63 2 1 51 0402 5% PCH_JTAG_TCK

RC66 2 1 51 0402 5% PCH_JTAG_TMS

RC69 2 1 51 0402 5% PCH_JTAG_TDI

RC72 2 1 51 0402 5% PCH_JTAG_TDO

RC75 2 1 51 0402 5% PCH_JTAGX

RC78 2 1 51 0402 5% PCH_JTAG_TCK

RC81 2 1 51 0402 5% PCH_JTAG_TMS

RC84 2 1 51 0402 5% PCH_JTAG_TDI

RC87 2 1 51 0402 5% PCH_JTAG_TDO

RC90 2 1 51 0402 5% PCH_JTAGX

RC93 2 1 51 0402 5% PCH_JTAG_TCK

RC96 2 1 51 0402 5% PCH_JTAG_TMS

RC99 2 1 51 0402 5% PCH_JTAG_TDI

RC102 2 1 51 0402 5% PCH_JTAG_TDO

RC105 2 1 51 0402 5% PCH_JTAGX

RC108 2 1 51 0402 5% PCH_JTAG_TCK

RC111 2 1 51 0402 5% PCH_JTAG_TMS

RC114 2 1 51 0402 5% PCH_JTAG_TDI

RC117 2 1 51 0402 5% PCH_JTAG_TDO

RC120 2 1 51 0402 5% PCH_JTAGX

RC123 2 1 51 0402 5% PCH_JTAG_TCK

RC126 2 1 51 0402 5% PCH_JTAG_TMS

RC129 2 1 51 0402 5% PCH_JTAG_TDI

RC132 2 1 51 0402 5% PCH_JTAG_TDO

RC135 2 1 51 0402 5% PCH_JTAGX

RC138 2 1 51 0402 5% PCH_JTAG_TCK

RC141 2 1 51 0402 5% PCH_JTAG_TMS

RC144 2 1 51 0402 5% PCH_JTAG_TDI

RC147 2 1 51 0402 5% PCH_JTAG_TDO

RC150 2 1 51 0402 5% PCH_JTAGX

RC153 2 1 51 0402 5% PCH_JTAG_TCK

RC156 2 1 51 0402 5% PCH_JTAG_TMS

RC159 2 1 51 0402 5% PCH_JTAG_TDI

RC162 2 1 51 0402 5% PCH_JTAG_TDO

RC165 2 1 51 0402 5% PCH_JTAGX

RC168 2 1 51 0402 5% PCH_JTAG_TCK

RC171 2 1 51 0402 5% PCH_JTAG_TMS

RC174 2 1 51 0402 5% PCH_JTAG_TDI

RC177 2 1 51 0402 5% PCH_JTAG_TDO

RC180 2 1 51 0402 5% PCH_JTAGX

RC183 2 1 51 0402 5% PCH_JTAG_TCK

RC186 2 1 51 0402 5% PCH_JTAG_TMS

RC189 2 1 51 0402 5% PCH_JTAG_TDI

RC192 2 1 51 0402 5% PCH_JTAG_TDO

RC195 2 1 51 0402 5% PCH_JTAGX

RC198 2 1 51 0402 5% PCH_JTAG_TCK

RC201 2 1 51 0402 5% PCH_JTAG_TMS

RC204 2 1 51 0402 5% PCH_JTAG_TDI

RC207 2 1 51 0402 5% PCH_JTAG_TDO

RC210 2 1 51 0402 5% PCH_JTAGX

RC213 2 1 51 0402 5% PCH_JTAG_TCK

RC216 2 1 51 0402 5% PCH_JTAG_TMS

RC219 2 1 51 0402 5% PCH_JTAG_TDI

RC222 2 1 51 0402 5% PCH_JTAG_TDO

RC225 2 1 51 0402 5% PCH_JTAGX

RC228 2 1 51 0402 5% PCH_JTAG_TCK

RC231 2 1 51 0402 5% PCH_JTAG_TMS

RC234 2 1 51 0402 5% PCH_JTAG_TDI

RC237 2 1 51 0402 5% PCH_JTAG_TDO

RC240 2 1 51 0402 5% PCH_JTAGX

RC243 2 1 51 0402 5% PCH_JTAG_TCK

RC246 2 1 51 0402 5% PCH_JTAG_TMS

RC249 2 1 51 0402 5% PCH_JTAG_TDI

RC252 2 1 51 0402 5% PCH_JTAG_TDO

RC255 2 1 51 0402 5% PCH_JTAGX

RC258 2 1 51 0402 5% PCH_JTAG_TCK

RC261 2 1 51 0402 5% PCH_JTAG_TMS

RC264 2 1 51 0402 5% PCH_JTAG_TDI

RC267 2 1 51 0402 5% PCH_JTAG_TDO

RC270 2 1 51 0402 5% PCH_JTAGX

RC273 2 1 51 0402 5% PCH_JTAG_TCK

RC276 2 1 51 0402 5% PCH_JTAG_TMS

RC279 2 1 51 0402 5% PCH_JTAG_TDI

RC282 2 1 51 0402 5% PCH_JTAG_TDO

RC285 2 1 51 0402 5% PCH_JTAGX

RC288 2 1 51 0402 5% PCH_JTAG_TCK

RC291 2 1 51 0402 5% PCH_JTAG_TMS

RC294 2 1 51 0402 5% PCH_JTAG_TDI

RC297 2 1 51 0402 5% PCH_JTAG_TDO

RC300 2 1 51 0402 5% PCH_JTAGX

RC303 2 1 51 0402 5% PCH_JTAG_TCK

RC306 2 1 51 0402 5% PCH_JTAG_TMS

RC309 2 1 51 0402 5% PCH_JTAG_TDI

RC312 2 1 51 0402 5% PCH_JTAG_TDO

RC315 2 1 51 0402 5% PCH_JTAGX

RC318 2 1 51 0402 5% PCH_JTAG_TCK

RC321 2 1 51 0402 5% PCH_JTAG_TMS

RC324 2 1 51 0402 5% PCH_JTAG_TDI

RC327 2 1 51 0402 5% PCH_JTAG_TDO

RC330 2 1 51 0402 5% PCH_JTAGX

RC333 2 1 51 0402 5% PCH_JTAG_TCK

RC336 2 1 51 0402 5% PCH_JTAG_TMS

RC339 2 1 51 0402 5% PCH_JTAG_TDI

RC342 2 1 51 0402 5% PCH_JTAG_TDO

RC345 2 1 51 0402 5% PCH_JTAGX

RC348 2 1 51 0402 5% PCH_JTAG_TCK

RC351 2 1 51 0402 5% PCH_JTAG_TMS

RC354 2 1 51 0402 5% PCH_JTAG_TDI

RC357 2 1 51 0402 5% PCH_JTAG_TDO

RC360 2 1 51 0402 5% PCH_JTAGX

RC363 2 1 51 0402 5% PCH_JTAG_TCK

RC366 2 1 51 0402 5% PCH_JTAG_TMS

RC369 2 1 51 0402 5% PCH_JTAG_TDI

RC372 2 1 51 0402 5% PCH_JTAG_TDO

RC375 2 1 51 0402 5% PCH_JTAGX

RC378 2 1 51 0402 5% PCH_JTAG_TCK

RC381 2 1 51 0402 5% PCH_JTAG_TMS

RC384 2 1 51 0402 5% PCH_JTAG_TDI

RC387 2 1 51 0402 5% PCH_JTAG_TDO

RC390 2 1 51 0402 5% PCH_JTAGX

RC393 2 1 51 0402 5% PCH_JTAG_TCK

RC396 2 1 51 0402 5% PCH_JTAG_TMS

RC399 2 1 51 0402 5% PCH_JTAG_TDI

RC402 2 1 51 0402 5% PCH_JTAG_TDO

RC405 2 1 51 0402 5% PCH_JTAGX

RC408 2 1 51 0402 5% PCH_JTAG_TCK

RC411 2 1 51 0402 5% PCH_JTAG_TMS

RC414 2 1 51 0402 5% PCH_JTAG_TDI

RC417 2 1 51 0402 5% PCH_JTAG_TDO

RC420 2 1 51 0402 5% PCH_JTAGX

RC423 2 1 51 0402 5% PCH_JTAG_TCK

RC426 2 1 51 0402 5% PCH_JTAG_TMS

RC429 2 1 51 0402 5% PCH_JTAG_TDI

RC432 2 1 51 0402 5% PCH_JTAG_TDO

RC435 2 1 51 0402 5% PCH_JTAGX

RC438 2 1 51 0402 5% PCH_JTAG_TCK

RC441 2 1 51 0402 5% PCH_JTAG_TMS

RC444 2 1 51 0402 5% PCH_JTAG_TDI

RC447 2 1 51 0402 5% PCH_JTAG_TDO

RC450 2 1 51 0402 5% PCH_JTAGX

RC453 2 1 51 0402 5% PCH_JTAG_TCK

RC456 2 1 51 0402 5% PCH_JTAG_TMS

RC459 2 1 51 0402 5% PCH_JTAG_TDI

RC462 2 1 51 0402 5% PCH_JTAG_TDO

RC465 2 1 51 0402 5% PCH_JTAGX

RC468 2 1 51 0402 5% PCH_JTAG_TCK

RC471 2 1 51 0402 5% PCH_JTAG_TMS

RC474 2 1 51 0402 5% PCH_JTAG_TDI

RC477 2 1 51 0402 5% PCH_JTAG_TDO

RC480 2 1 51 0402 5% PCH_JTAGX

RC483 2 1 51 0402 5% PCH_JTAG_TCK

RC486 2 1 51 0402 5% PCH_JTAG_TMS

RC489 2 1 51 0402 5% PCH_JTAG_TDI

RC492 2 1 51 0402 5% PCH_JTAG_TDO

RC495 2 1 51 0402 5% PCH_JTAGX

RC498 2 1 51 0402 5% PCH_JTAG_TCK

RC501 2 1 51 0402 5% PCH_JTAG_TMS

RC504 2 1 51 0402 5% PCH_JTAG_TDI

RC507 2 1 51 0402 5% PCH_JTAG_TDO

RC510 2 1 51 0402 5% PCH_JTAGX

RC513 2 1 51 0402 5% PCH_JTAG_TCK

RC516 2 1 51 0402 5% PCH_JTAG_TMS

RC519 2 1 51 0402 5% PCH_JTAG_TDI

RC522 2 1 51 0402 5% PCH_JTAG_TDO

RC525 2 1 51 0402 5% PCH_JTAGX

RC528 2 1 51 0402 5% PCH_JTAG_TCK

RC531 2 1 51 0402 5% PCH_JTAG_TMS

RC534 2 1 51 0402 5% PCH_JTAG_TDI

RC537 2 1 51 0402 5% PCH_JTAG_TDO

RC540 2 1 51 0402 5% PCH_JTAGX

RC543 2 1 51 0402 5% PCH_JTAG_TCK

RC546 2 1 51 0402 5% PCH_JTAG_TMS

RC549 2 1 51 0402 5% PCH_JTAG_TDI

RC552 2 1 51 0402 5% PCH_JTAG_TDO

RC555 2 1 51 0402 5% PCH_JTAGX

RC558 2 1 51 0402 5% PCH_JTAG_TCK

RC561 2 1 51 0402 5% PCH_JTAG_TMS

RC564 2 1 51 0402 5% PCH_JTAG_TDI

RC567 2 1 51 0402 5% PCH_JTAG_TDO

RC570 2 1 51 0402 5% PCH_JTAGX

RC573 2 1 51 0402 5% PCH_JTAG_TCK

RC576 2 1 51 0402 5% PCH_JTAG_TMS

RC579 2 1 51 0402 5% PCH_JTAG_TDI

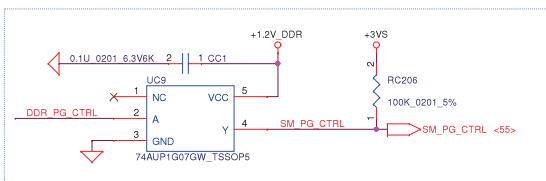
RC582 2 1 51 0402 5% PCH_JTAG_TDO

RC585 2 1 51 0402 5% PCH_JTAGX

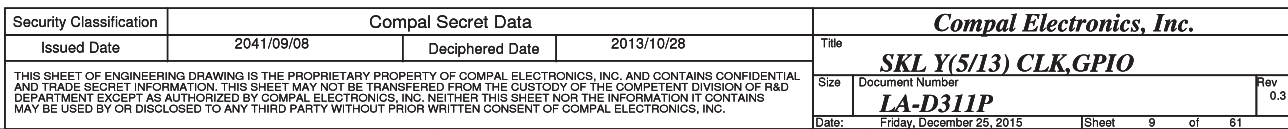
RC588 2 1 51 0402 5% PCH_JTAG_TCK

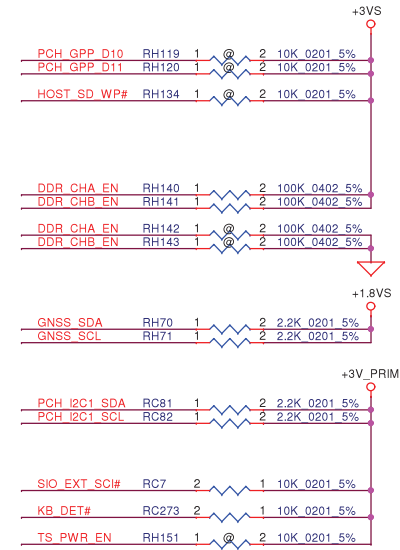
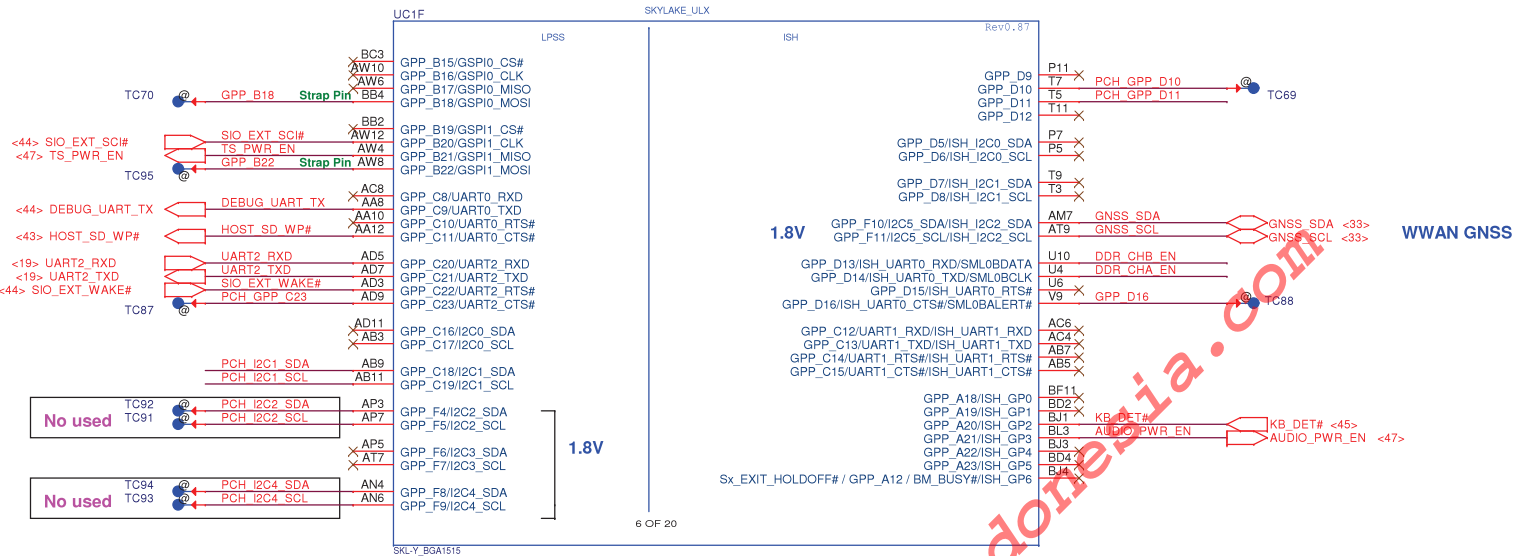
RC591 2 1 51 0402 5% PCH_JTAG_TMS

Non-Interleave Memory



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				SKL Y(2/13) DDRIII			
				Size	Document Number	Rev	
				LA-D311P		0.3	
Date:				Friday, December 25, 2015		Sheet	6 of 61



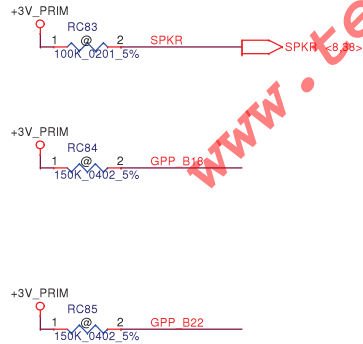


Functional Strap Definitions

GPP_B14 (Internal Pull Down): SPKR
TOP Swap Override
0 = Disable TOP Swap mode.----> AAU30 Use
1 = Enable TOP Swap Mode.

GPP_B18 (Internal Pull Down): GSSPIO_MOSI
No Reboot
0 = Disable No Reboot mode. --> AAU30 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GPP_B22 (Internal Pull Down): GSSPI1_MOSI
Boot BIOS Strap Bit
0 = SPI Mode --> AAU30 Use
1 = LPC Mode



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						Size	Document Number			Rev	
						LA-D311P					0.3
Date:						Friday, December 25, 2015		Sheet	10 of 61		

TBT

WLAN

WiGig

NGFF SSD

Cardreader

HCA

UC1H

SKYLAKE_ULX

Rev0.87

SSIC / USB3

PCIe/USB3/SATA

USB2

8 OF 20

SKL-Y_BGA1515

closed MCP 1000 mils

closed MCP 2000 mils

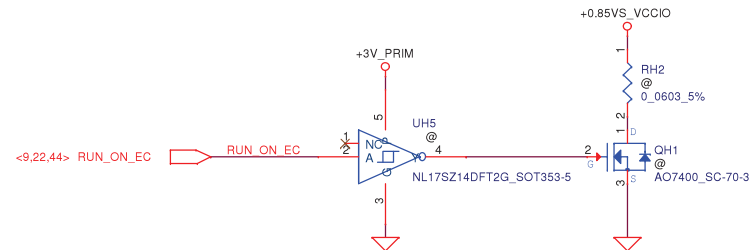
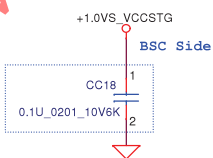
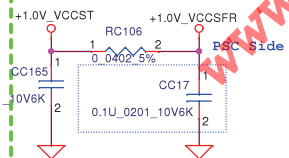
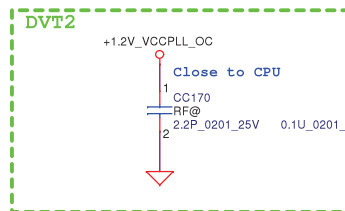
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Size	Document Number	Rev		0.3	
LA-D311P		Date		Friday, December 25, 2015	
Sheet		11		of 51	

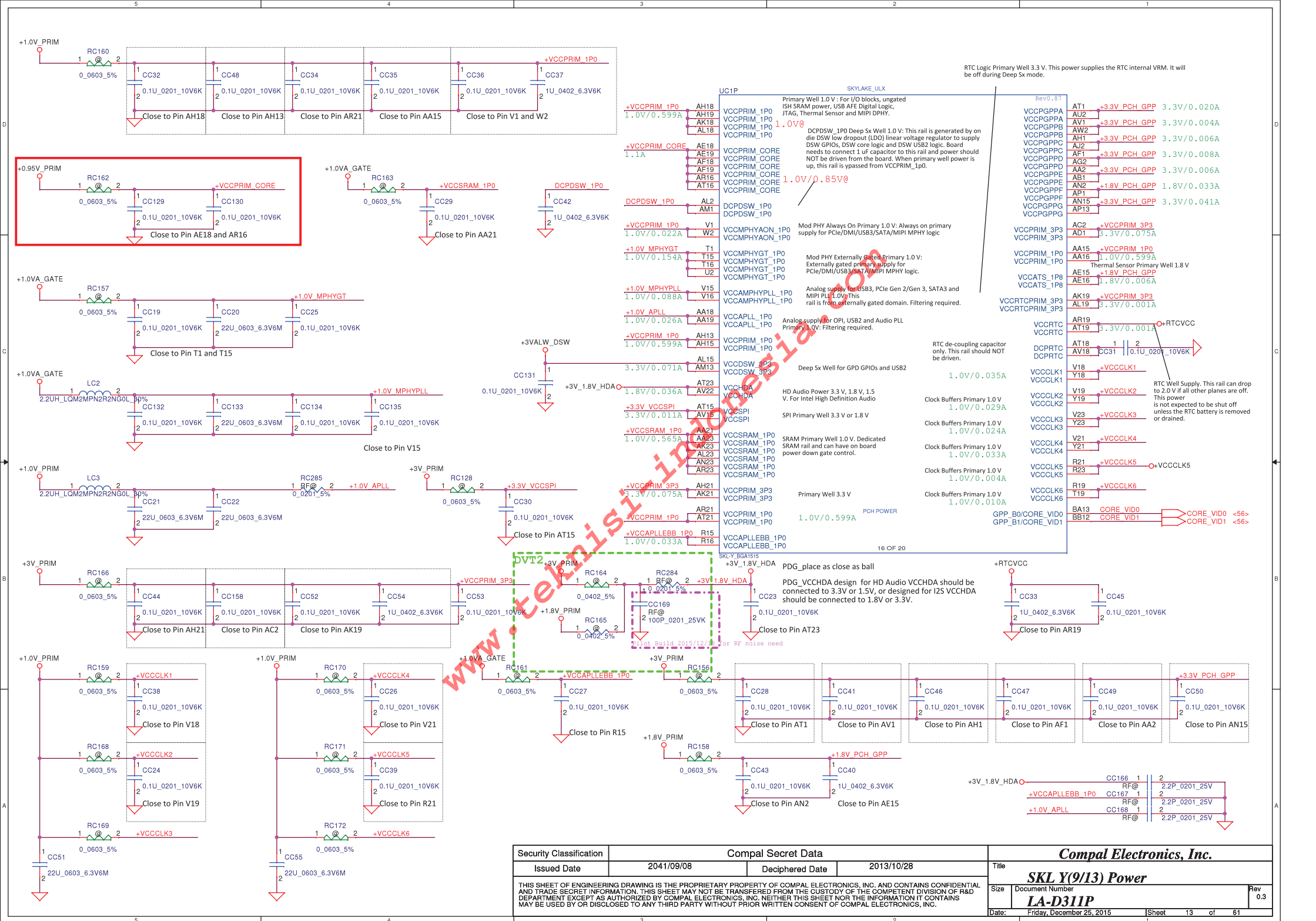
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Total etch length
= 186.94mils
PDG P597

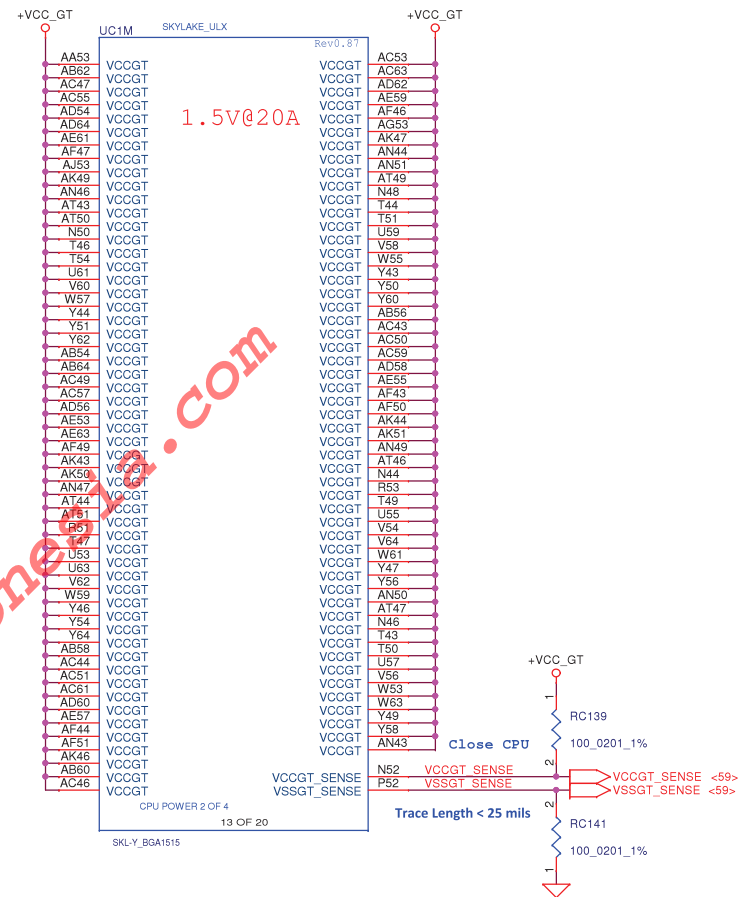
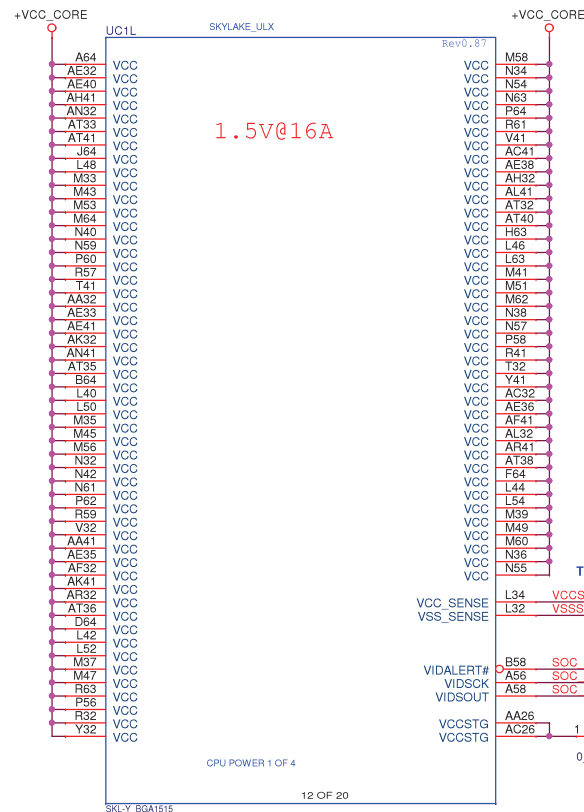
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VCCSTG : Gated sustain voltage for processor standby modes

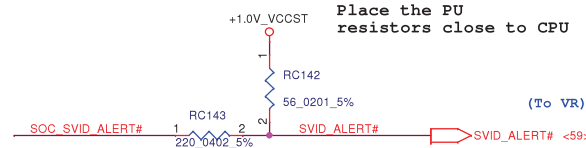


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				Date	Friday, December 25, 2015
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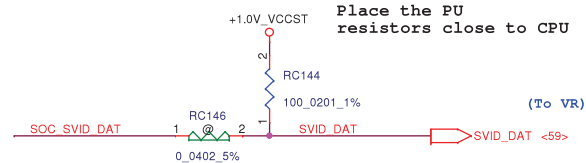




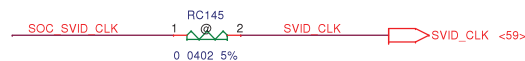
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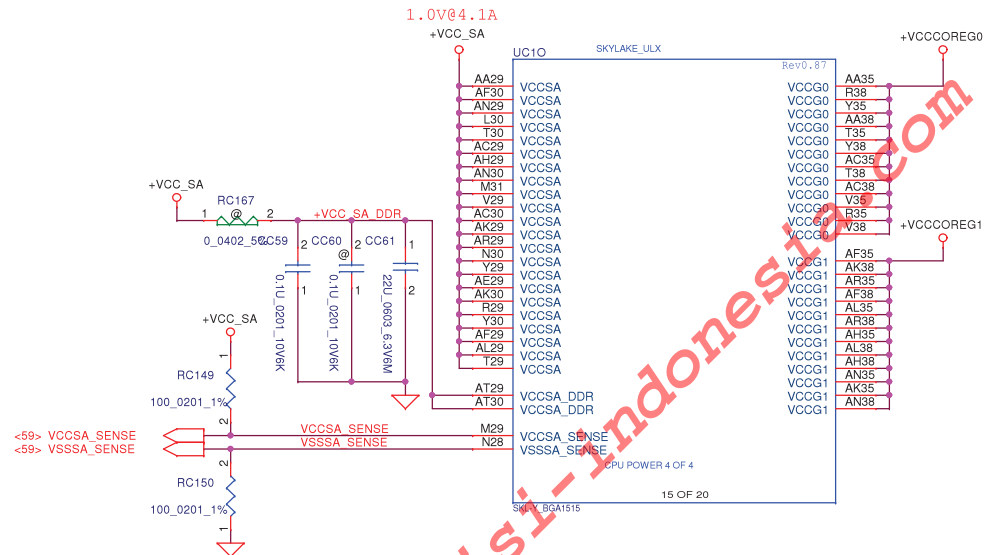
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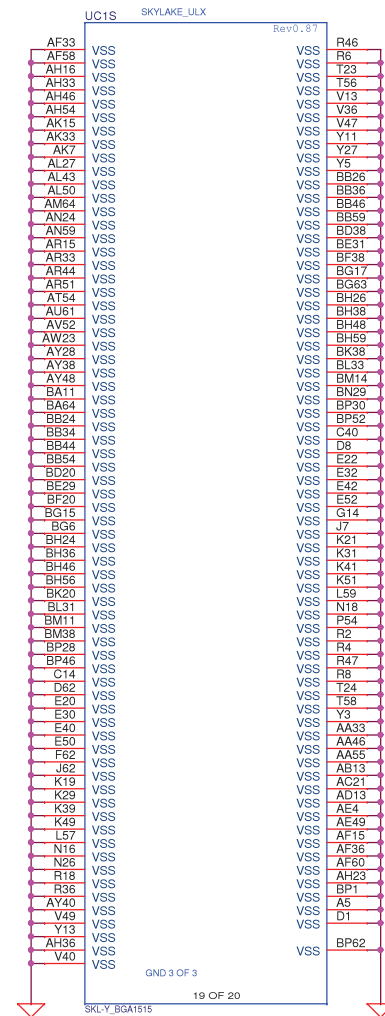
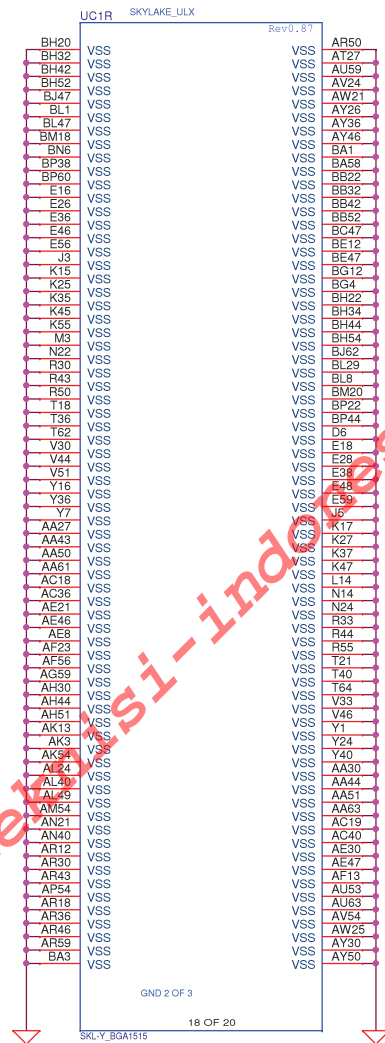
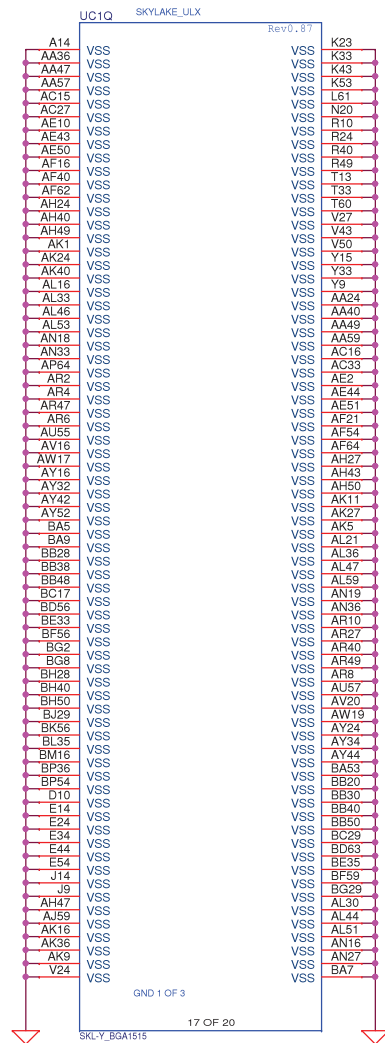
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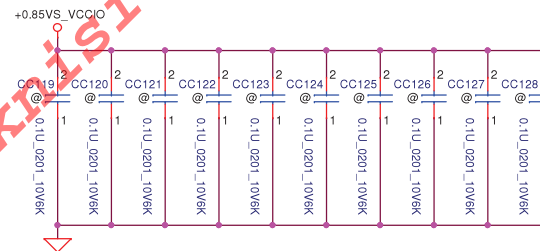
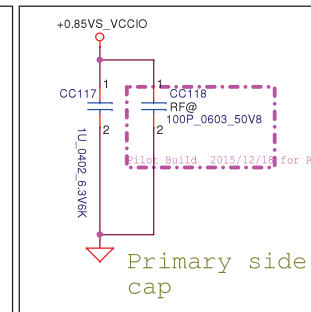
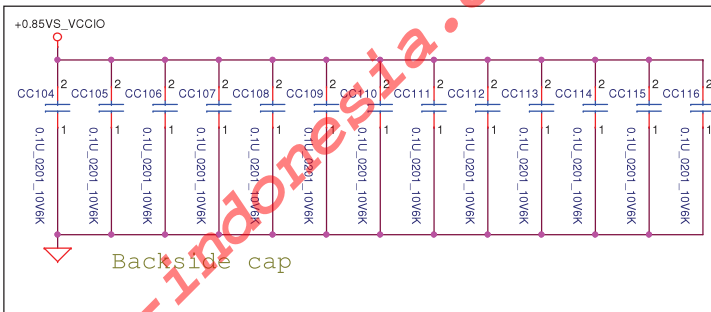
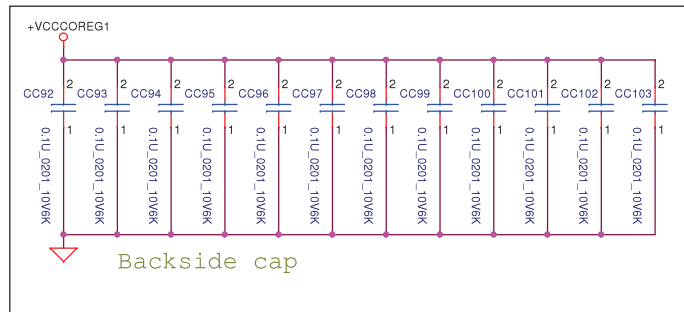
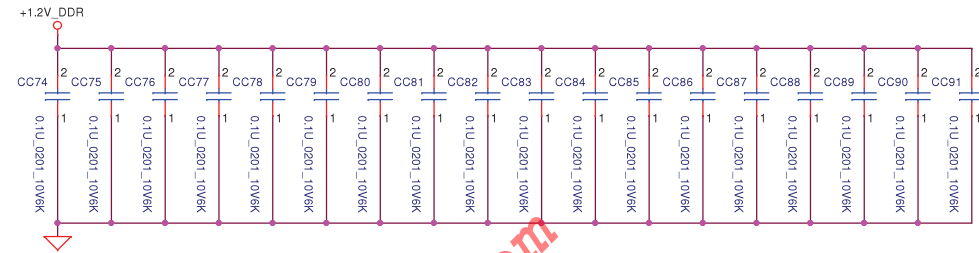
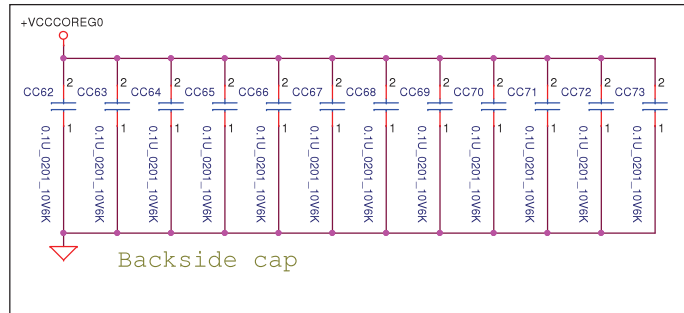
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Size	Document Number	Date		Sheet	Rev
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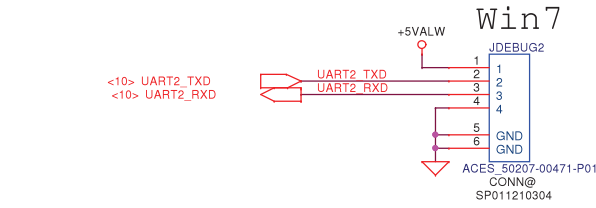


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				Date:	Friday, December 25, 2015
				Sheet	16 of 51
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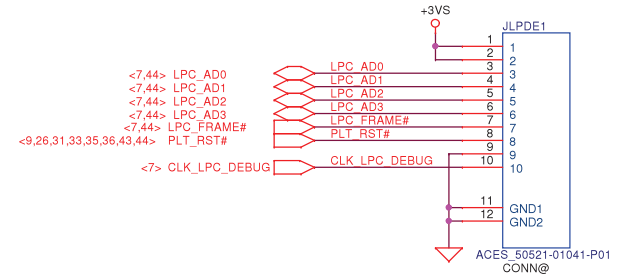


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Size	Document Number	Rev		LA-D311P	
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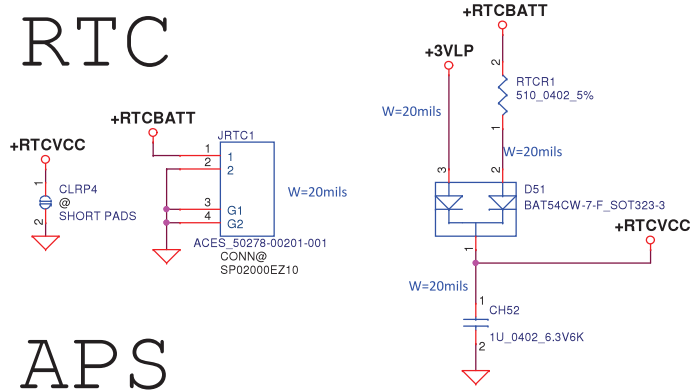
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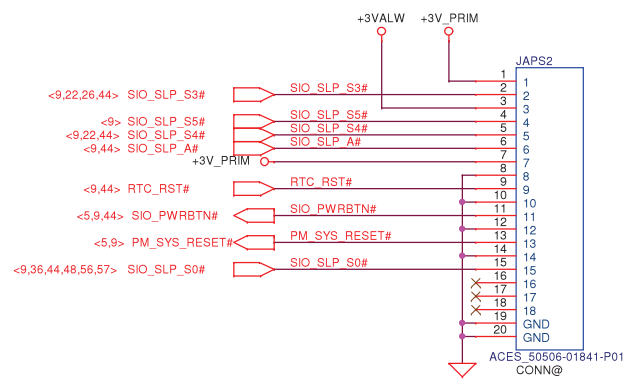
BIOS debug



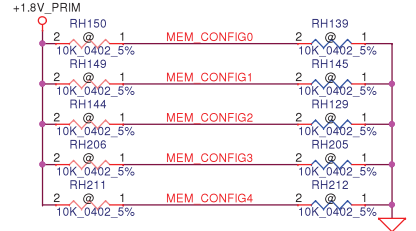
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APS



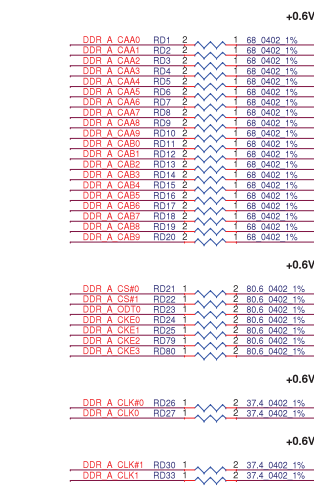
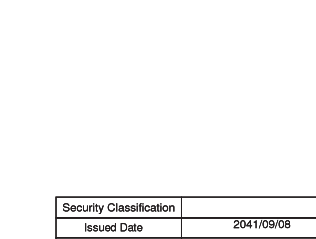
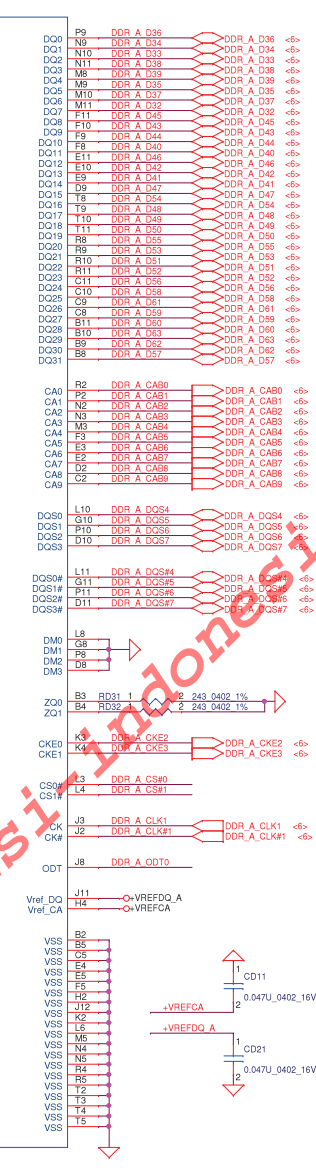
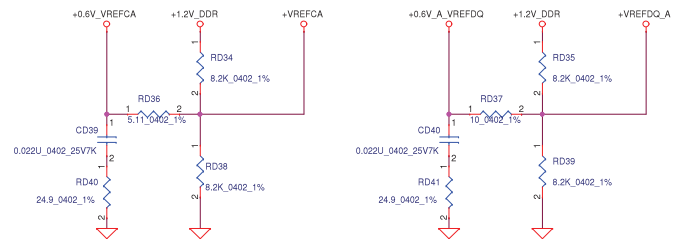
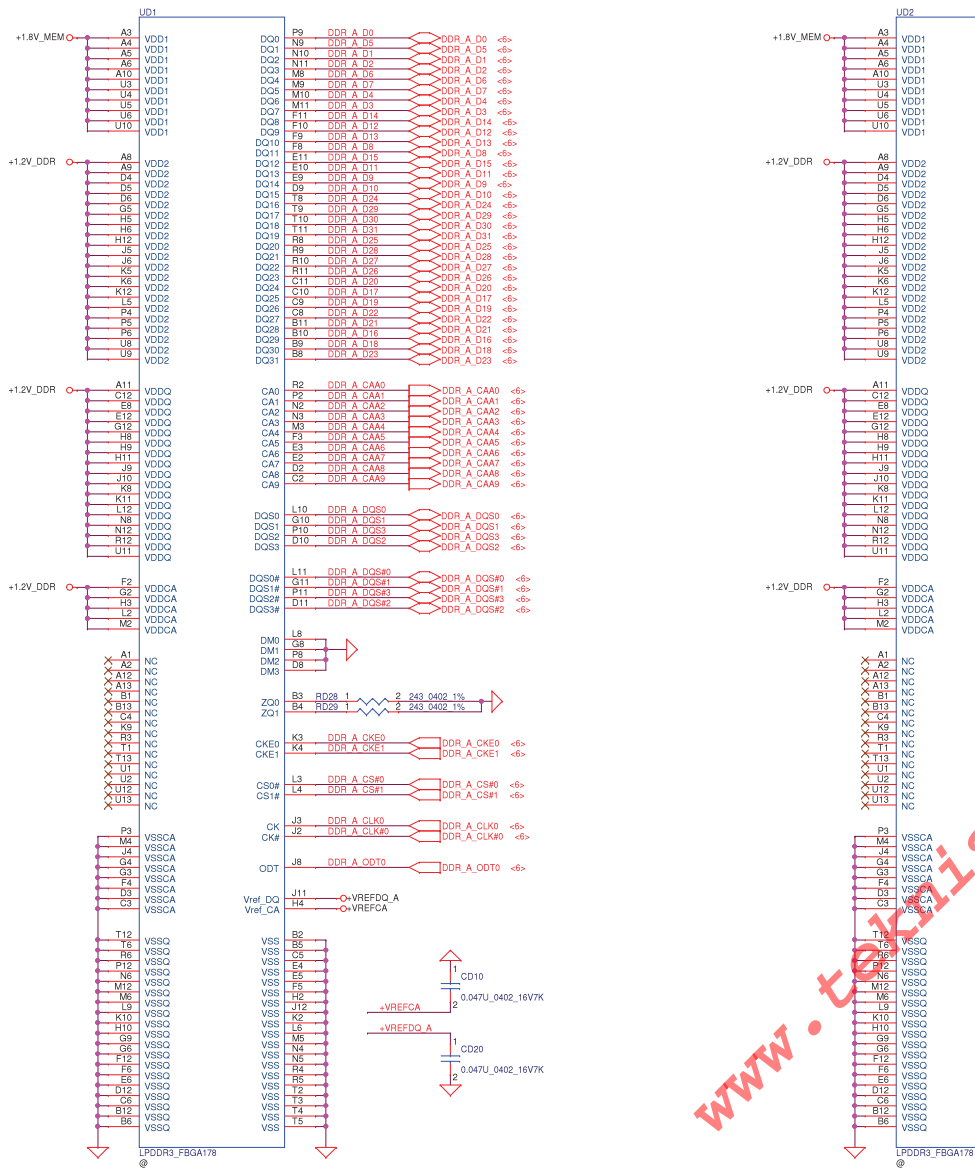
DDR Memory Configuratio Type Strap pin



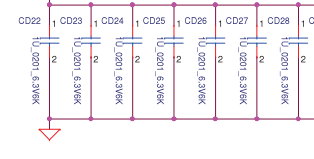
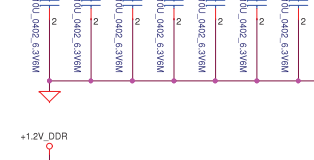
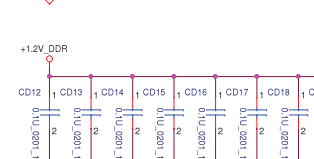
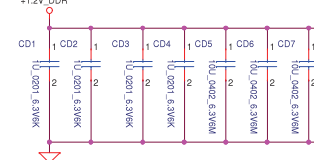
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MEM_CONFIG0	0	1	0	1	0	1	0	1	0
MEM_CONFIG1	0	0	1	1	0	0	1	0	0
MEM_CONFIG2	0	0	0	0	1	1	0	0	0
MEM_CONFIG3	0	0	0	0	0	0	0	0	1
MEM_CONFIG4	0	0	0	0	0	0	0	0	0

DRAM Option					DRAM Config Option					X76
					MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3	MEM_CONFIG4	
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Micron 8G/1866					<input type="checkbox"/> X76_M8G@ UD1 EDFA232A2MA-JD-F-R A3 SA00008Q11L	<input type="checkbox"/> X76_M8G@ UD2 EDFA232A2MA-JD-F-R A3 SA00008Q11L	<input type="checkbox"/> X76_M8G@ UD3 EDFA232A2MA-JD-F-R A3 SA00008Q11L	<input type="checkbox"/> X76_M8G@ UD4 EDFA232A2MA-JD-F-R A3 SA00008Q11L	<input type="checkbox"/> X76_M8G@ UD5 EDFA232A2MA-JD-F-R A3 SA00008Q11L	X7666031L06
Micron 16G/1866					<input type="checkbox"/> X76_M16G@ UD1 EDFA232A1MA-JD-F-R A3 SA00008QW1L	<input type="checkbox"/> X76_M16G@ UD2 EDFA232A1MA-JD-F-R A3 SA00008QW1L	<input type="checkbox"/> X76_M16G@ UD3 EDFA232A1MA-JD-F-R A3 SA00008QW1L	<input type="checkbox"/> X76_M16G@ UD4 EDFA232A1MA-JD-F-R A3 SA00008QW1L	<input type="checkbox"/> X76_M16G@ UD5 EDFA232A1MA-JD-F-R A3 SA00008QW1L	X7666031L09
Hynix 4G/1866					<input type="checkbox"/> X76_H4G@ UD1 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	<input type="checkbox"/> X76_H4G@ UD2 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	<input type="checkbox"/> X76_H4G@ UD3 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	<input type="checkbox"/> X76_H4G@ UD4 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	<input type="checkbox"/> X76_H4G@ UD5 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	X7666031L01
Hynix 8G/1866					<input type="checkbox"/> X76_H8G@ UD1 H9CCNNN8GTMLAR-NUD A3 SA00008FJ1L	<input type="checkbox"/> X76_H8G@ UD2 H9CCNNN8GTMLAR-NUD A3 SA00008FJ1L	<input type="checkbox"/> X76_H8G@ UD3 H9CCNNN8GTMLAR-NUD A3 SA00008FJ1L	<input type="checkbox"/> X76_H8G@ UD4 H9CCNNN8GTMLAR-NUD A3 SA00008FJ1L	<input type="checkbox"/> X76_H8G@ UD5 H9CCNNN8GTMLAR-NUD A3 SA00008FJ1L	X7666031L04
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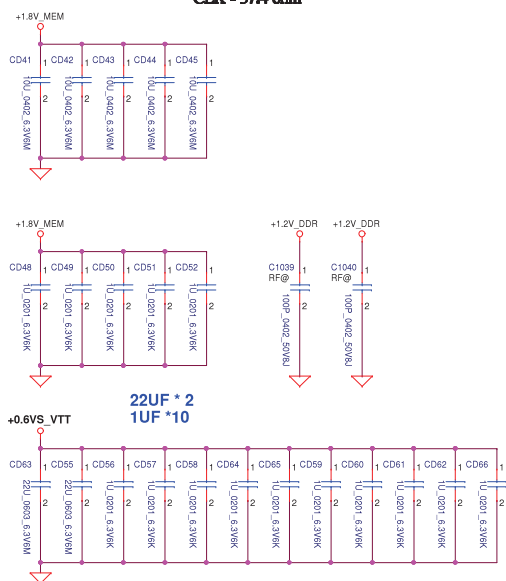
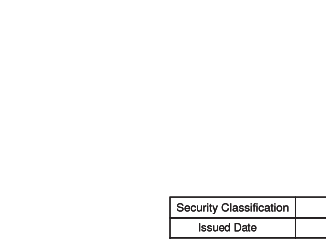
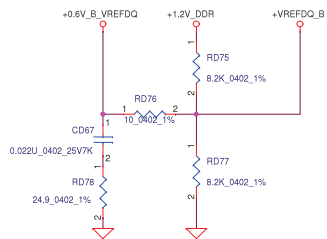
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Issued Date	2041/09/08	Deciphered Date	2013/10/28	RTC,Debug, RAM setting	
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					LA-D311P
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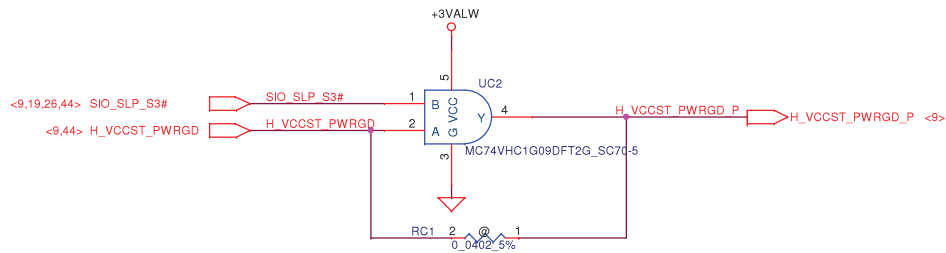
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CS/CKE/ODT - 80.6 ohm
CLK - 37.4 ohm



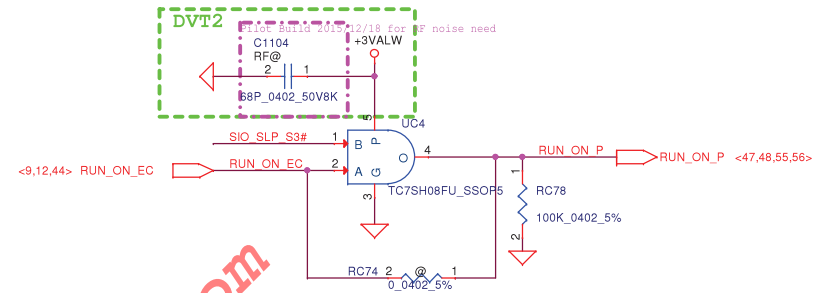
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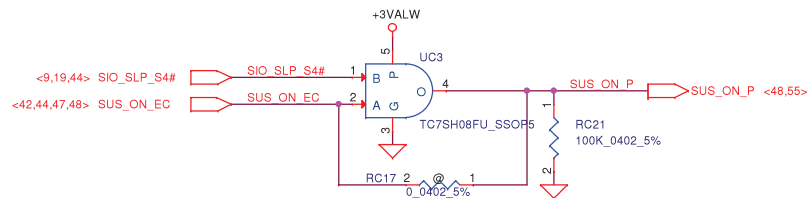
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Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title	LPDDRIII Channel B	
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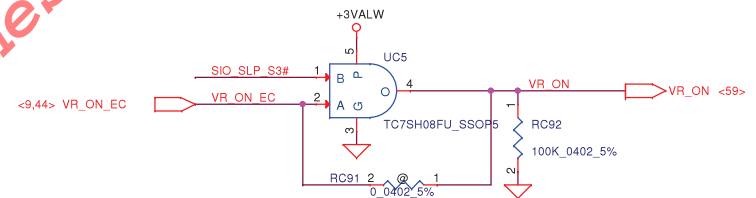
Change CPU VCCST_PWRGD enable from EC & PCH
H_VCCST_PWRGD (3.3V), H_VCCST_PWRGD_P (1.0V)
If need to mount RC1, need to add level shift.



Change VCCIO & VCCSTG power enable from EC & PCH



Change VCCST & 1.2_VR power enable from EC & PCH

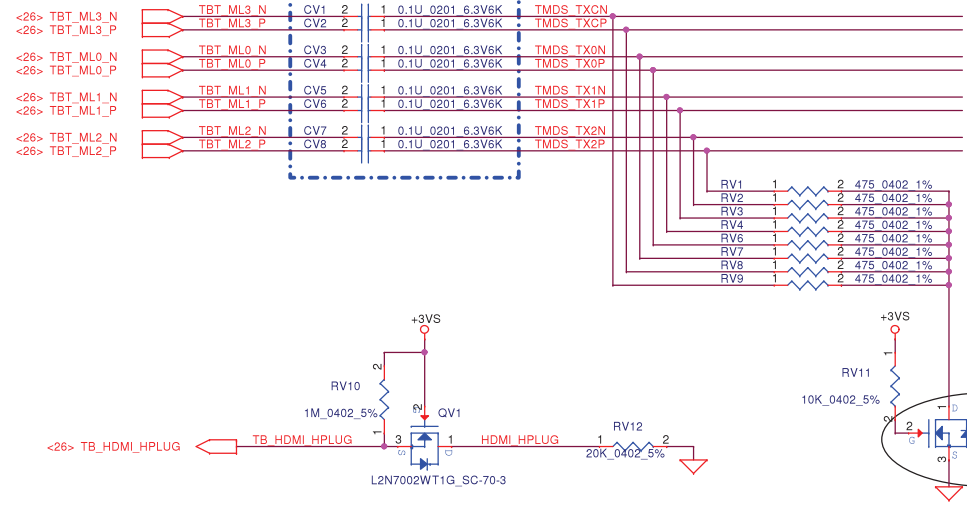


Change VCORE power enable from EC & PCH

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Size	Document Number	LA-D311P		Rev 0.3	
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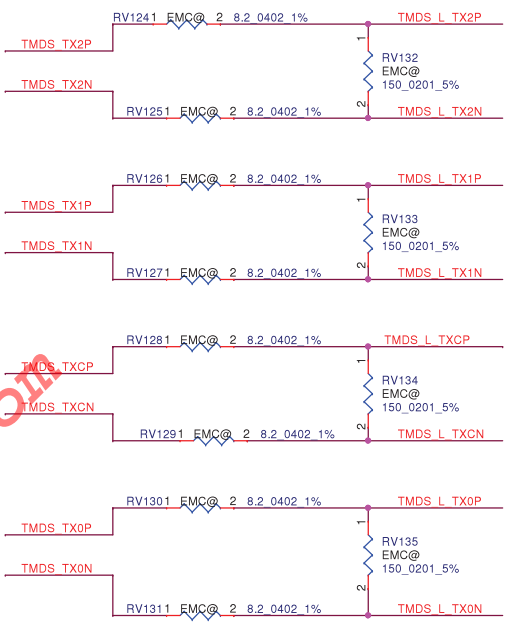
HDMI Active Level Shift (ALS type)

1014: Steg change to 0201 package.



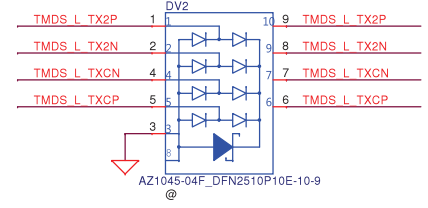
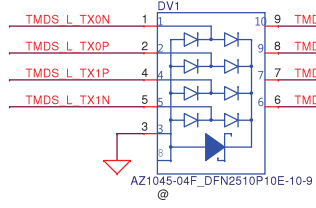
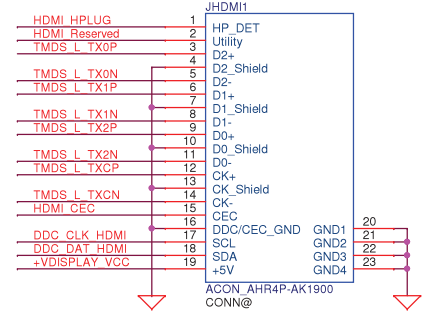
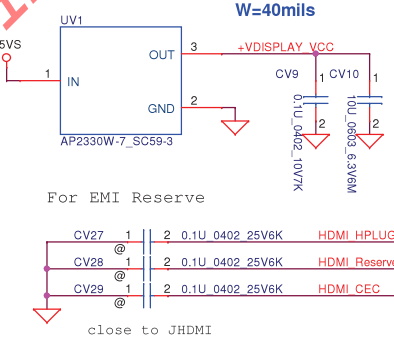
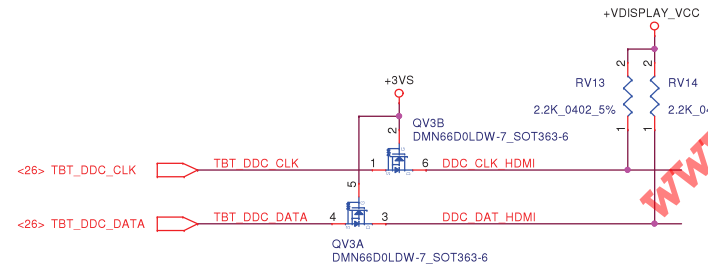
Place close to JHDMI1

For EMI



HDMI DDC

HDMI Conn

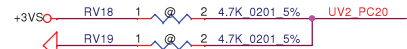
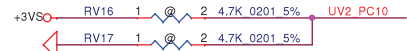


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Chip operational mode configuration;
Internal pull down at ~150K Ω , 3.3V I/O.

```
L: Control switching mode (default)
H: Automatic switching mode
```



AUX interception disable for Port y (y=1,2)
Internal pull down at ~150K?, 3.3V I/O.

```
L: AUX interception enable, driver configuration
   is set by link training (default)
H: AUX interception disable, driver output with
   fixed 800mv and 0dB
M: AUX interception disable, driver output with
   fixed 400mv and 0dB
```

DP_MUX_SEL pin

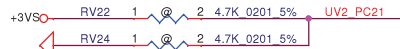
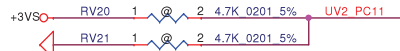
Port switching control or priority configuration;
Internal pull down at ~150K Ω , 3.3V I/O.

L: Port1 is selected or with higher priority
(default)
H: Port2 is selected or with higher priority



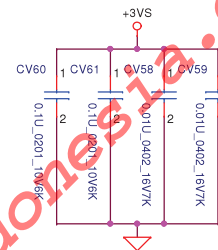
Automatic EQ disable;
Internal pull down at ~150K?, 3.3V IO

```
L: Automatic EQ enable (default)
H: Automatic EQ disable
```

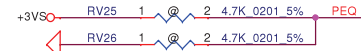


Output swing adjustment for Port y (y=1,2).
Internal pull down at ~150K?, 3.3V I/O.

```
L:default
H: +20%
M: -16.7%
```

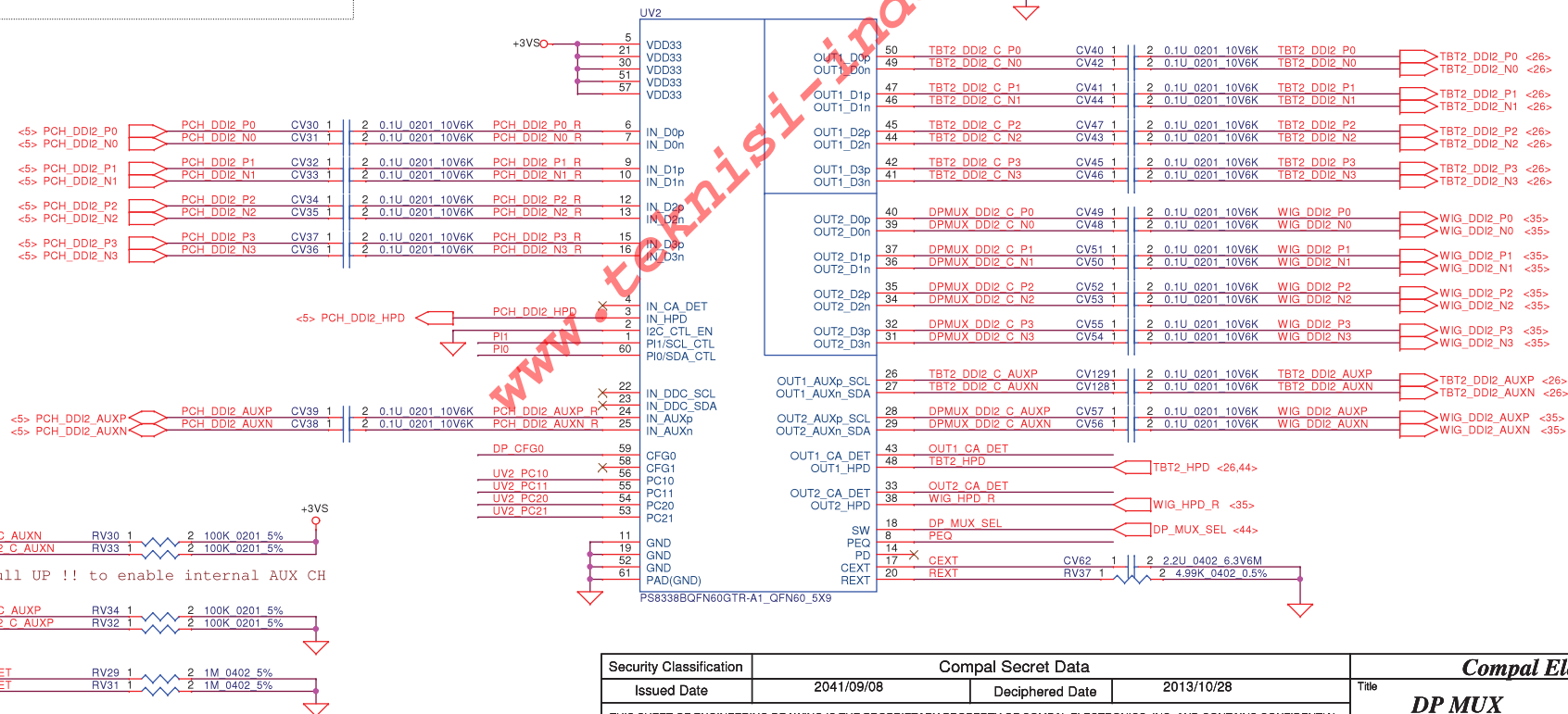


```
Auto test enable;
Internal pull down at ~150K?, 3.3V I/O.
L: Auto test disable & input offset cancellation
  enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable
```

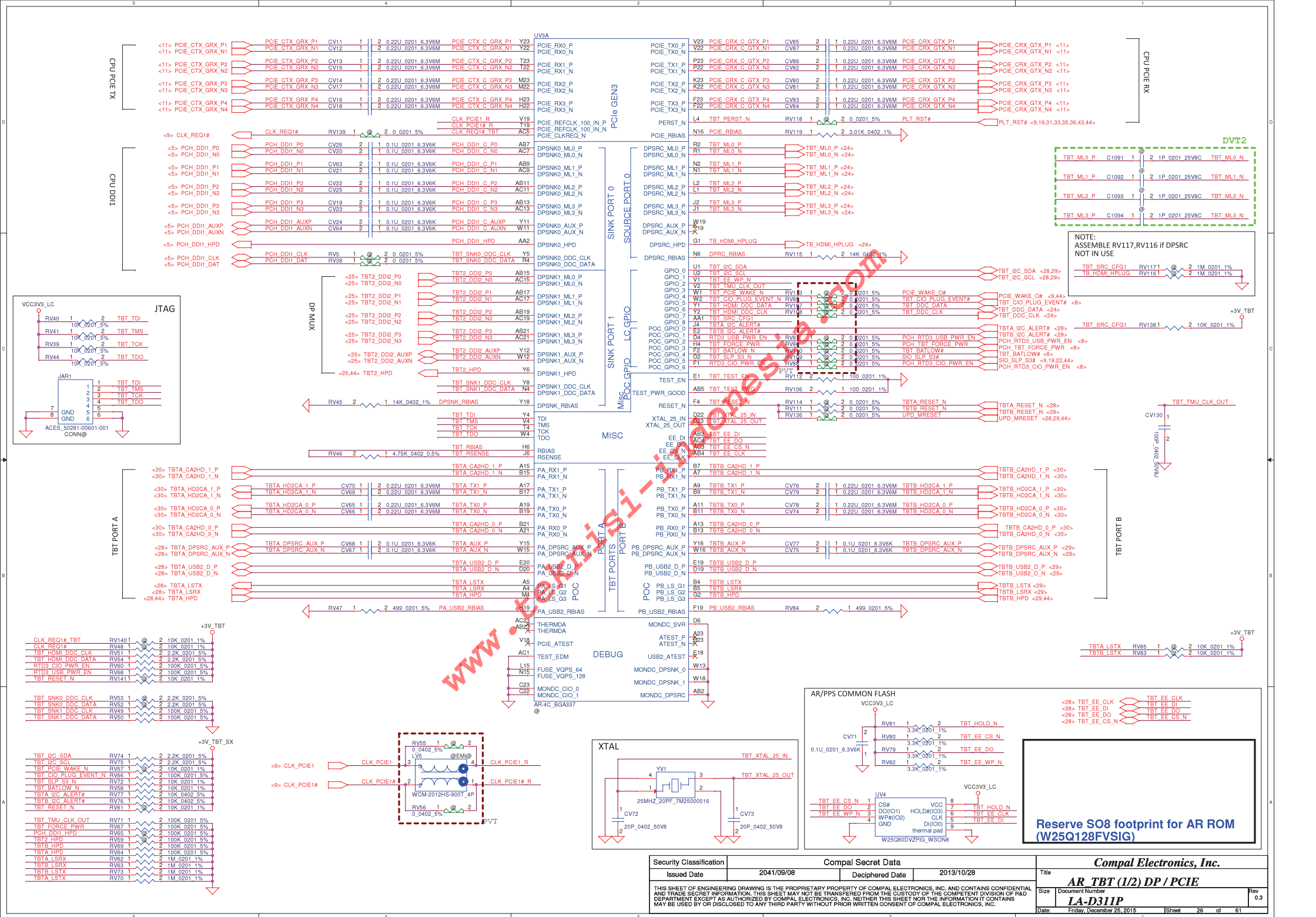


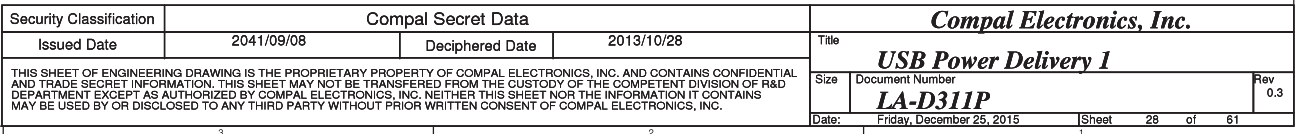
Programmable input equalization levels; Internal pull down at ~150K Ω , 3.3V I/O.

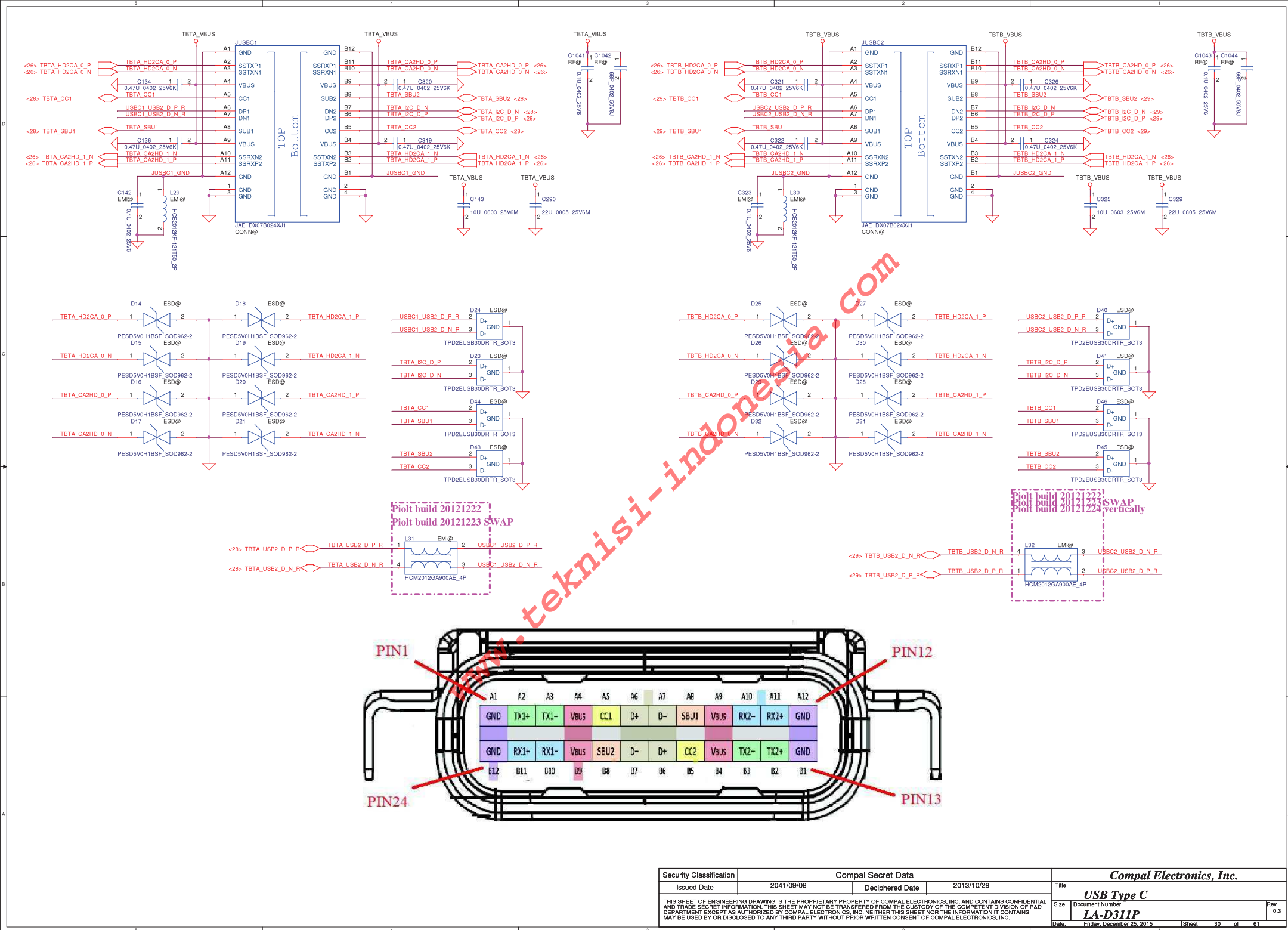
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2



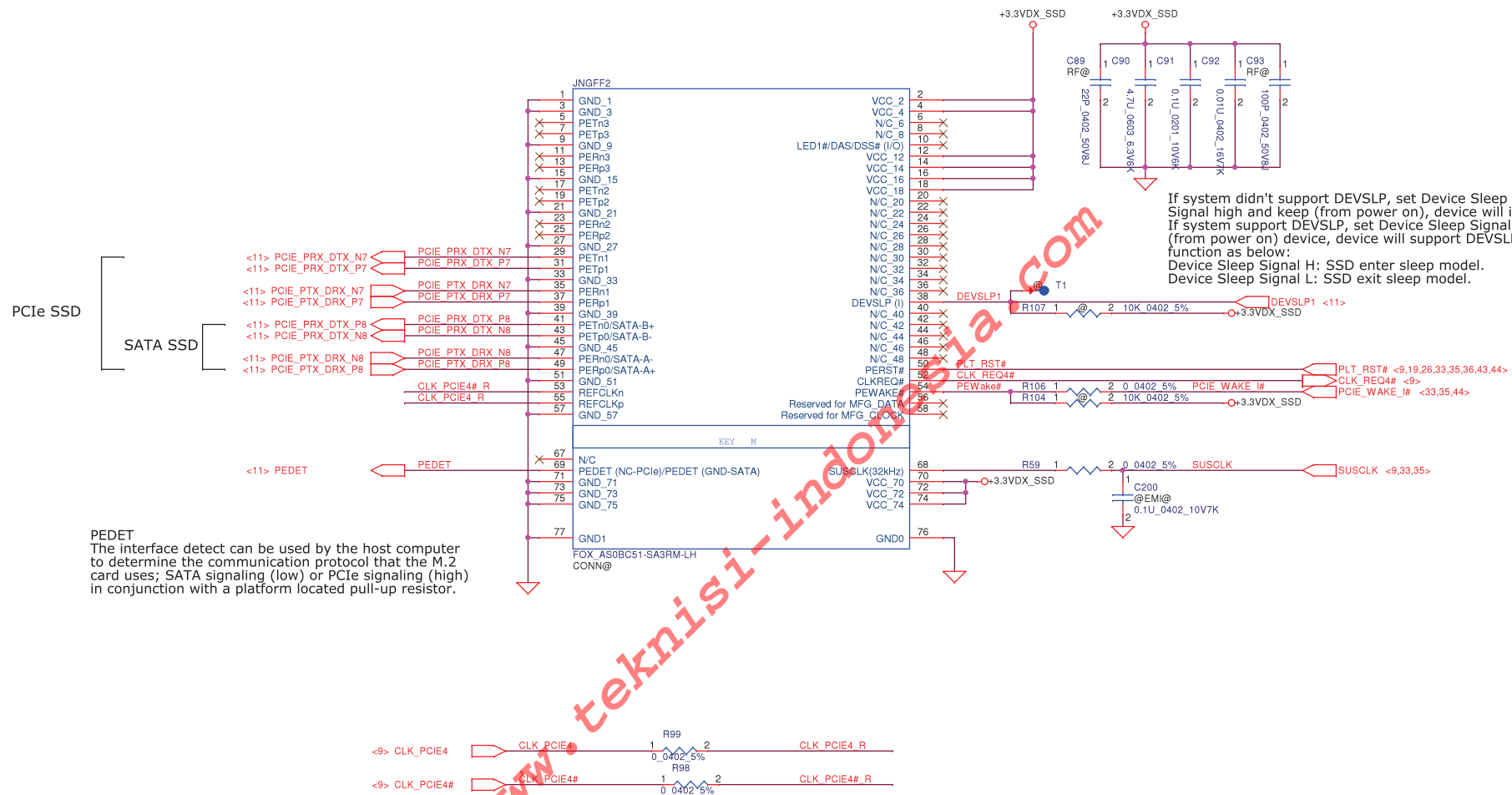
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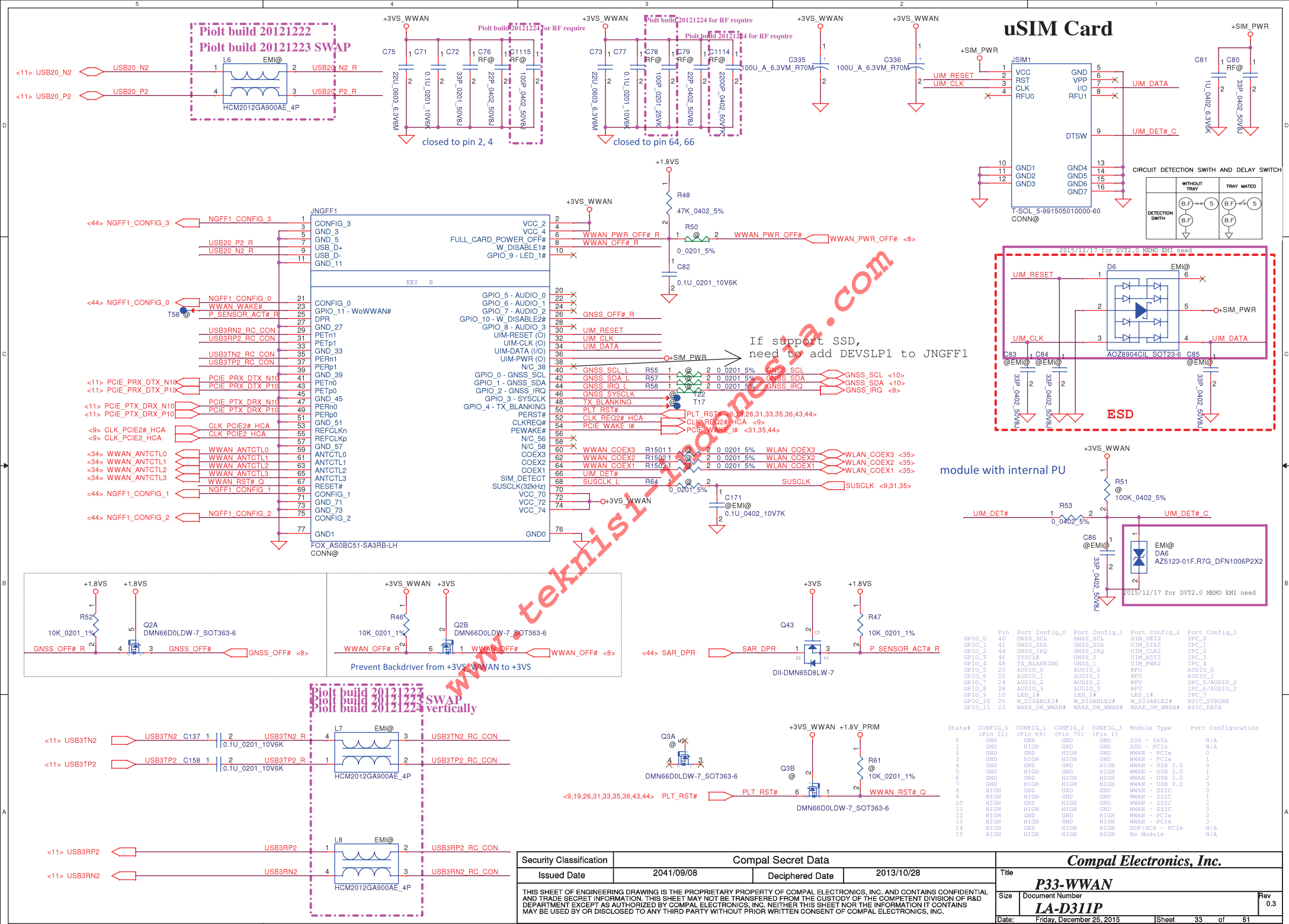
NGFF(SATA)



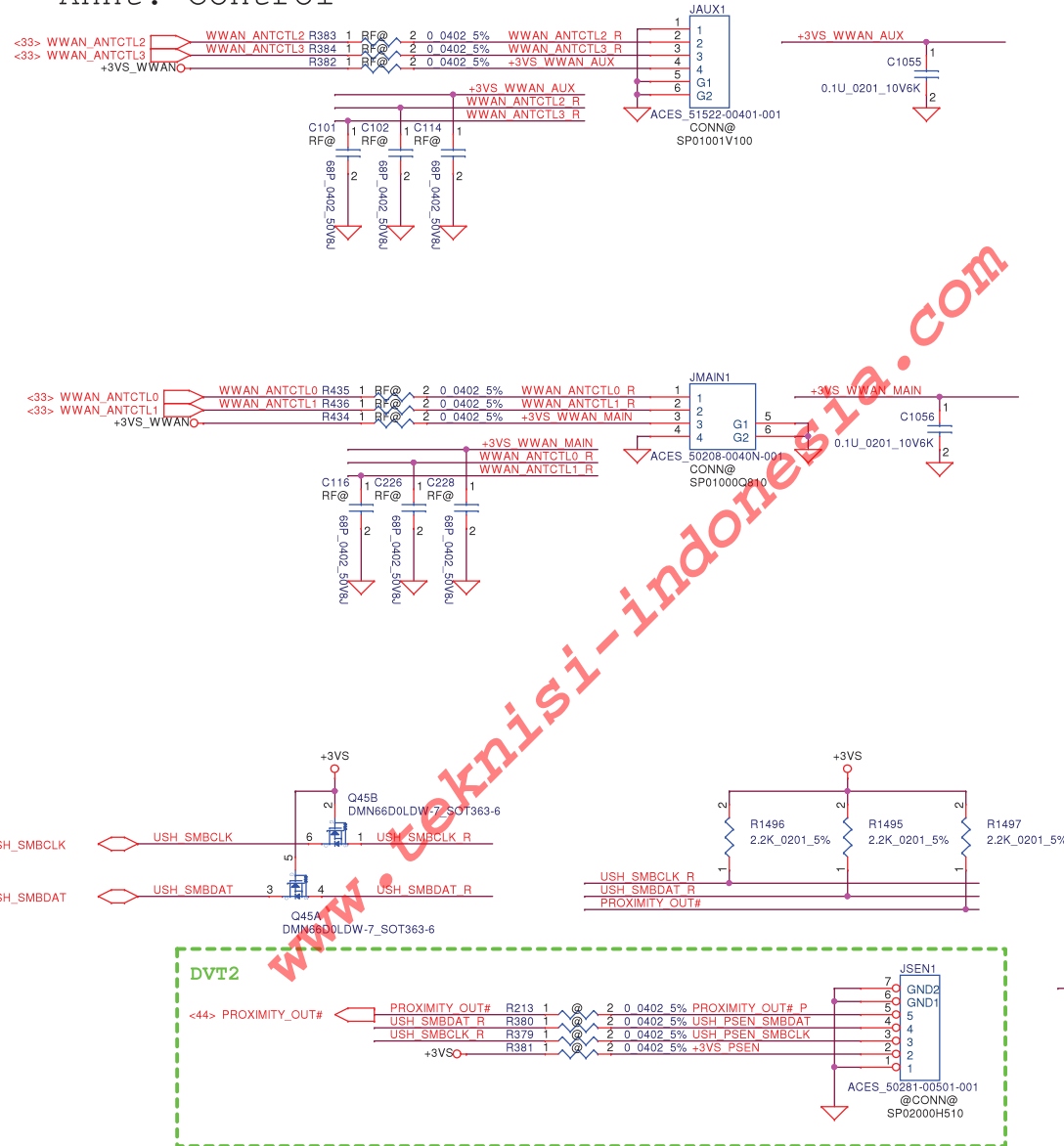
Security Classification		Compal Secret Data		Title	
Issued Date	2041/09/08	Deciphered Date	2013/10/28	SATA SSD	
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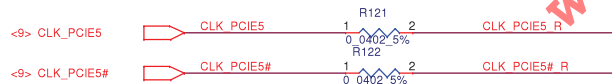
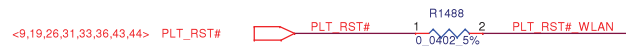
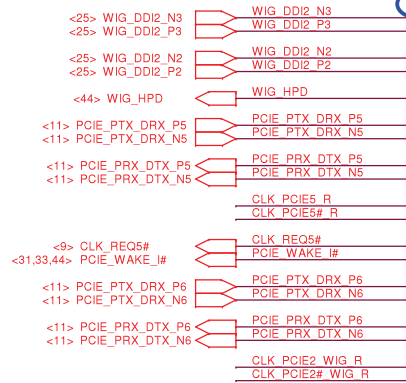
Annt. Control



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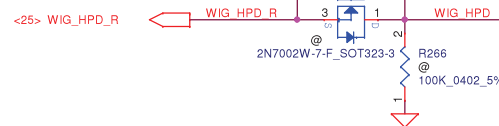
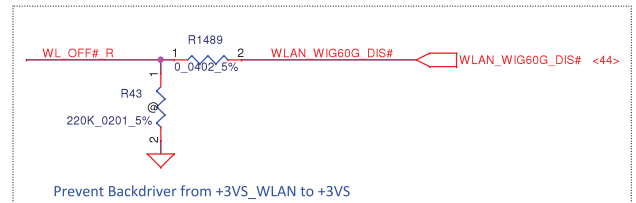
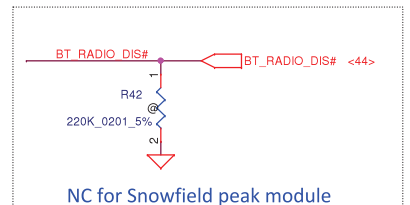
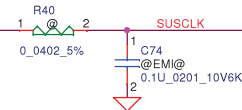
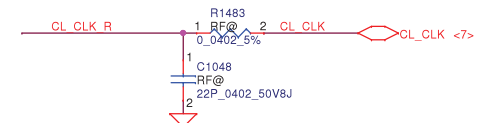
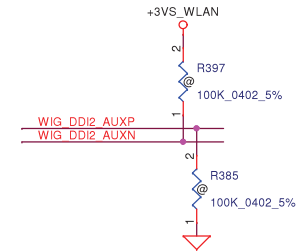
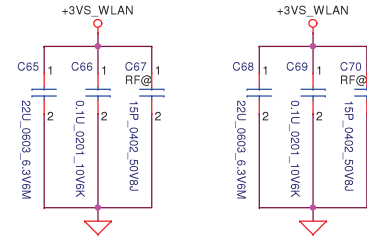


for KEY-A module this pin
should be NC, not GND



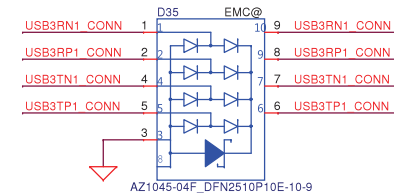
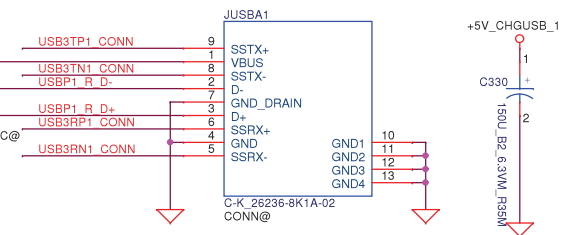
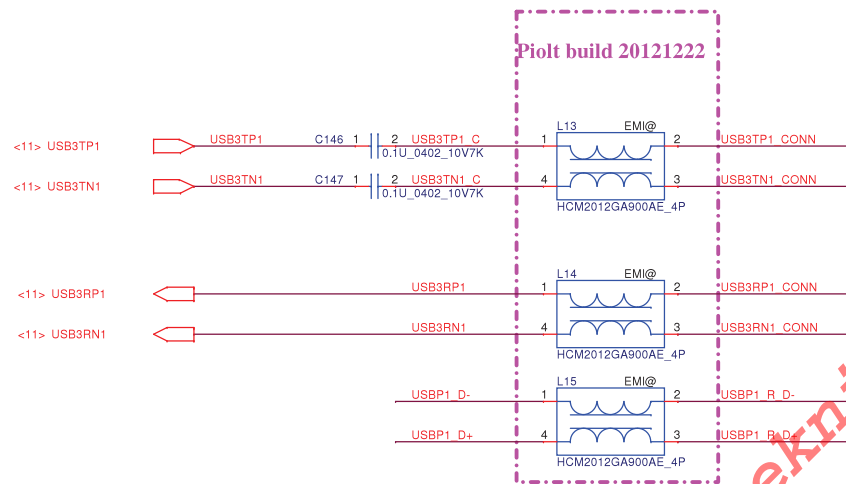
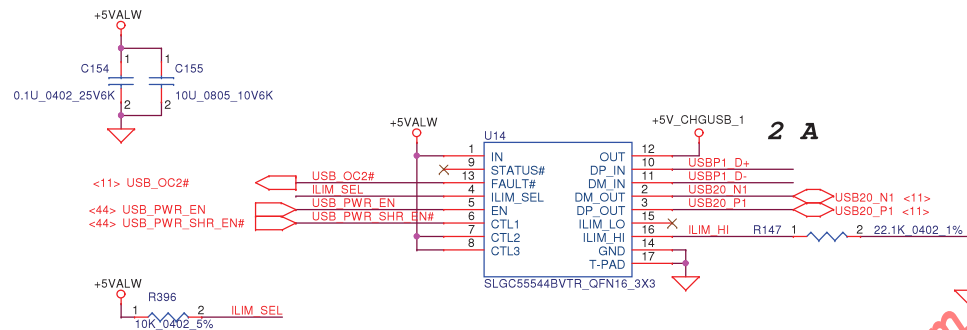
closed to pin 2, 4

closed to pin 64, 66

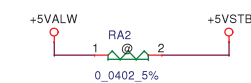
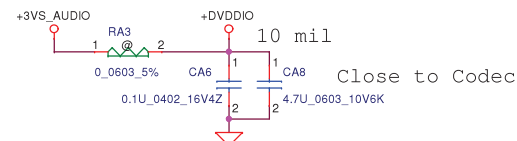
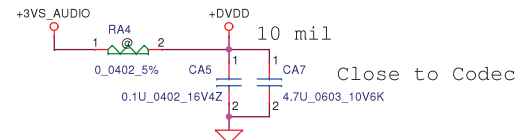
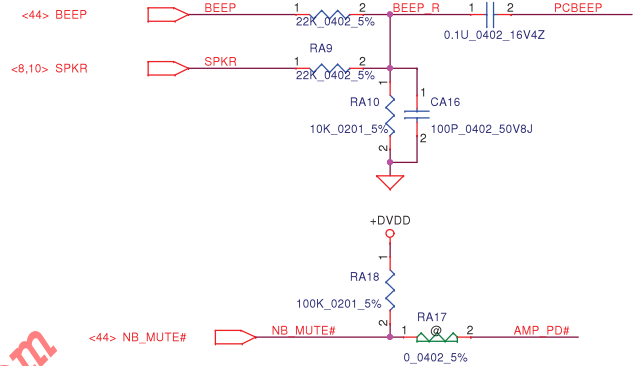
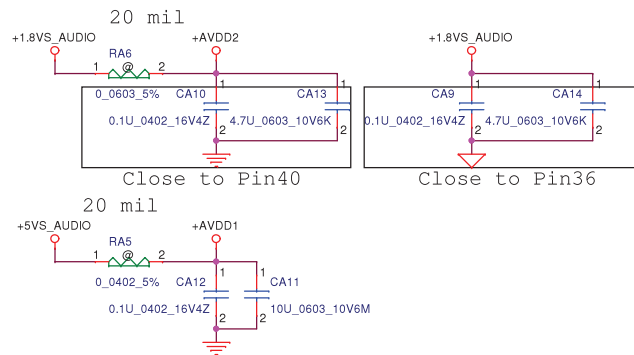
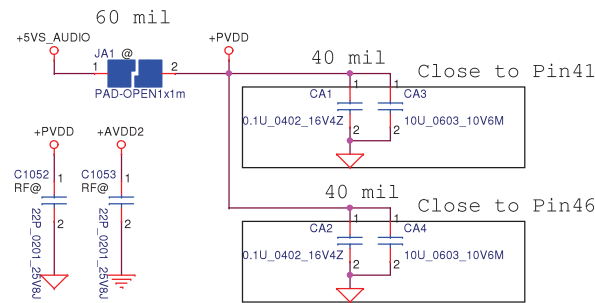


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A



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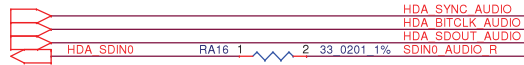


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<8> HDA_BITCLK_AUDIO

<8> HDA_SDOUT_AUDIO

<8> HDA_SDIN0



<46> DMIC_DAT_CODECD

<46> DMIC_CLK_CODECD

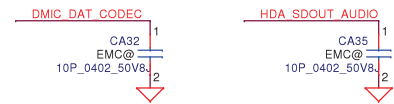
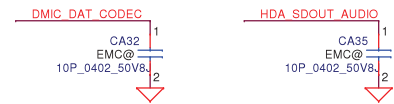
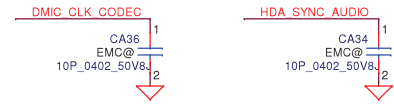
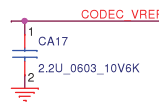
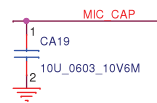
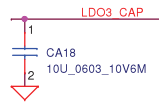
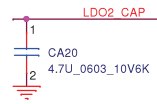
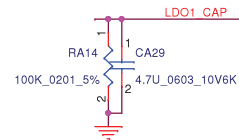
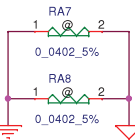
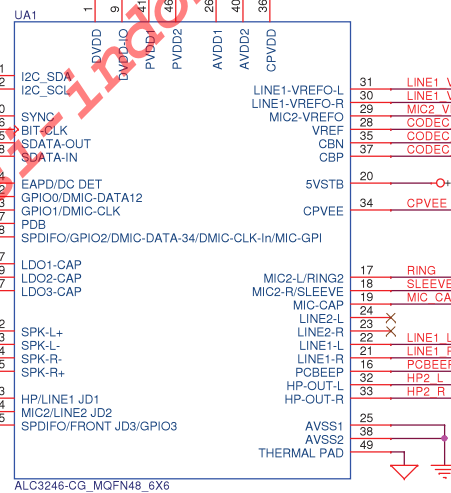
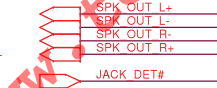


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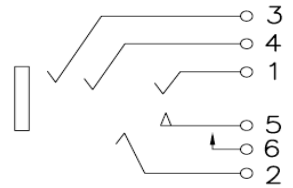
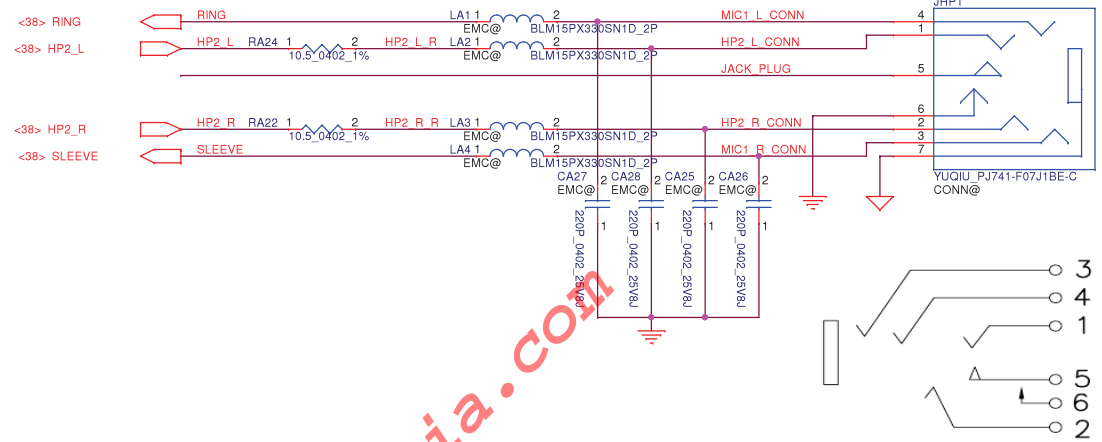
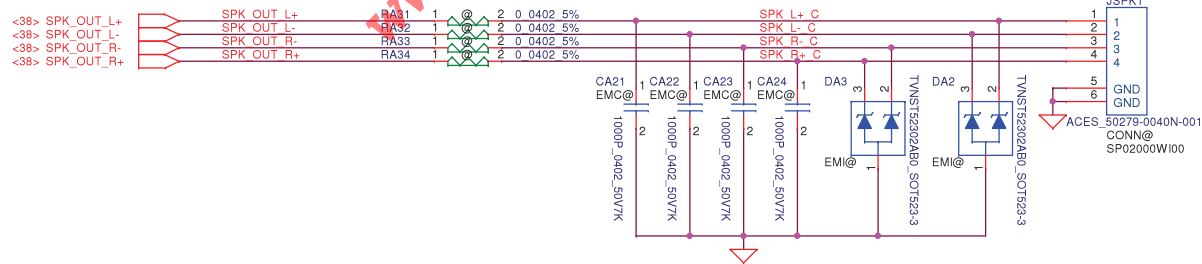
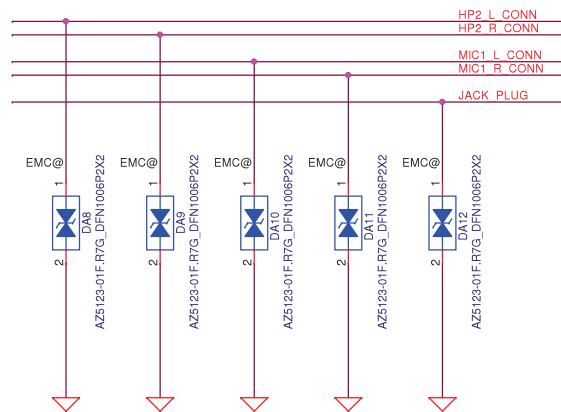
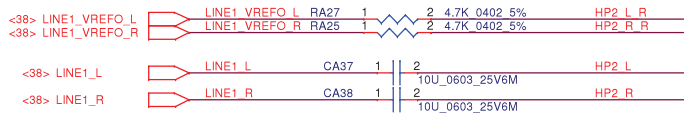
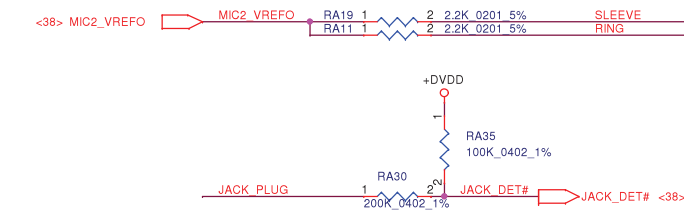
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<39> SPK_OUT_R-

<39> SPK_OUT_R+

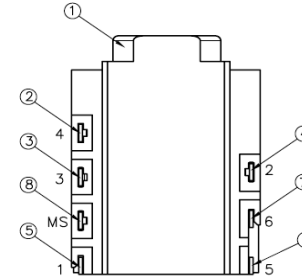


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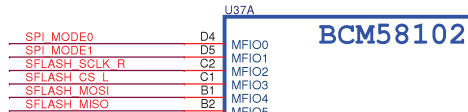
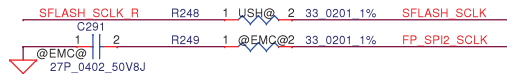


SCHEMATIC

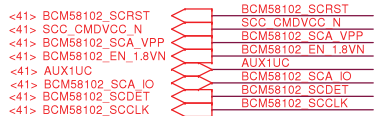
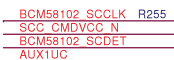
NO.	PART NAME	TER'NO.
10	SEPARATOR	
9	MYLAR	
8	SHIELD	
7	BREAK TERMINAL	6
6	TRANSFER TERMINAL	5
5	TIP TERMINAL	1
4	RING B TERMINAL	2
3	RING A TERMINAL	3
2	EARTH TERMINAL	4
1	HOUSING	



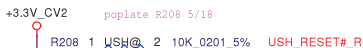
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Size		Document Number		Rev	
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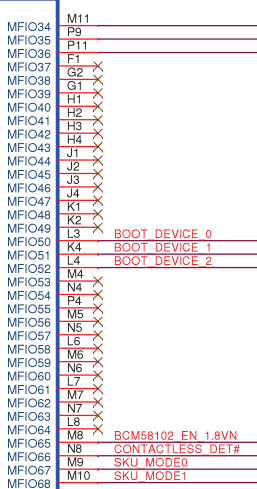
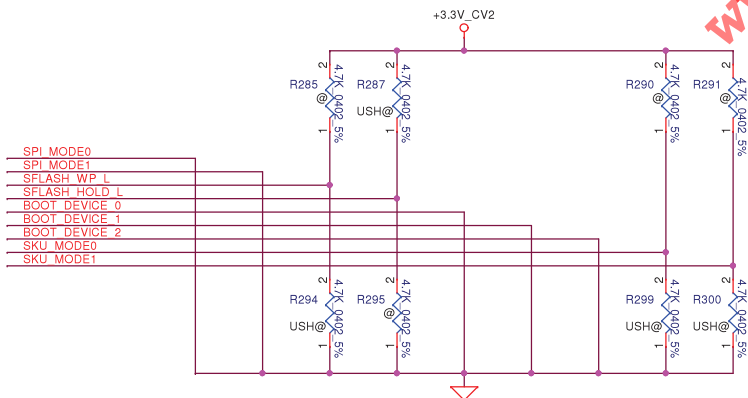
Change USH_SPI2_SS to FP_SPI2_SS 5/18



Remove U43, R387 5/18

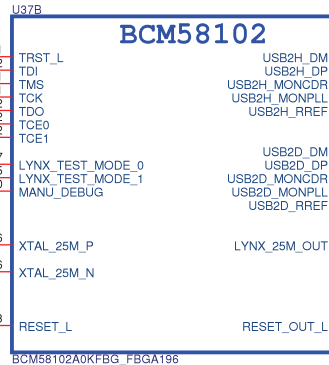
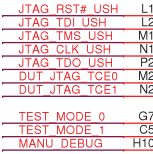


remove R386 5/18



+3.3V_CV2

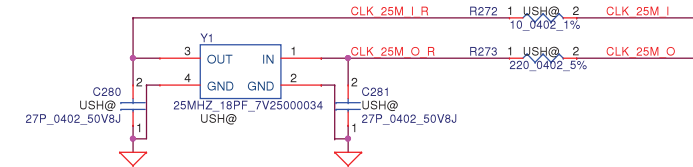
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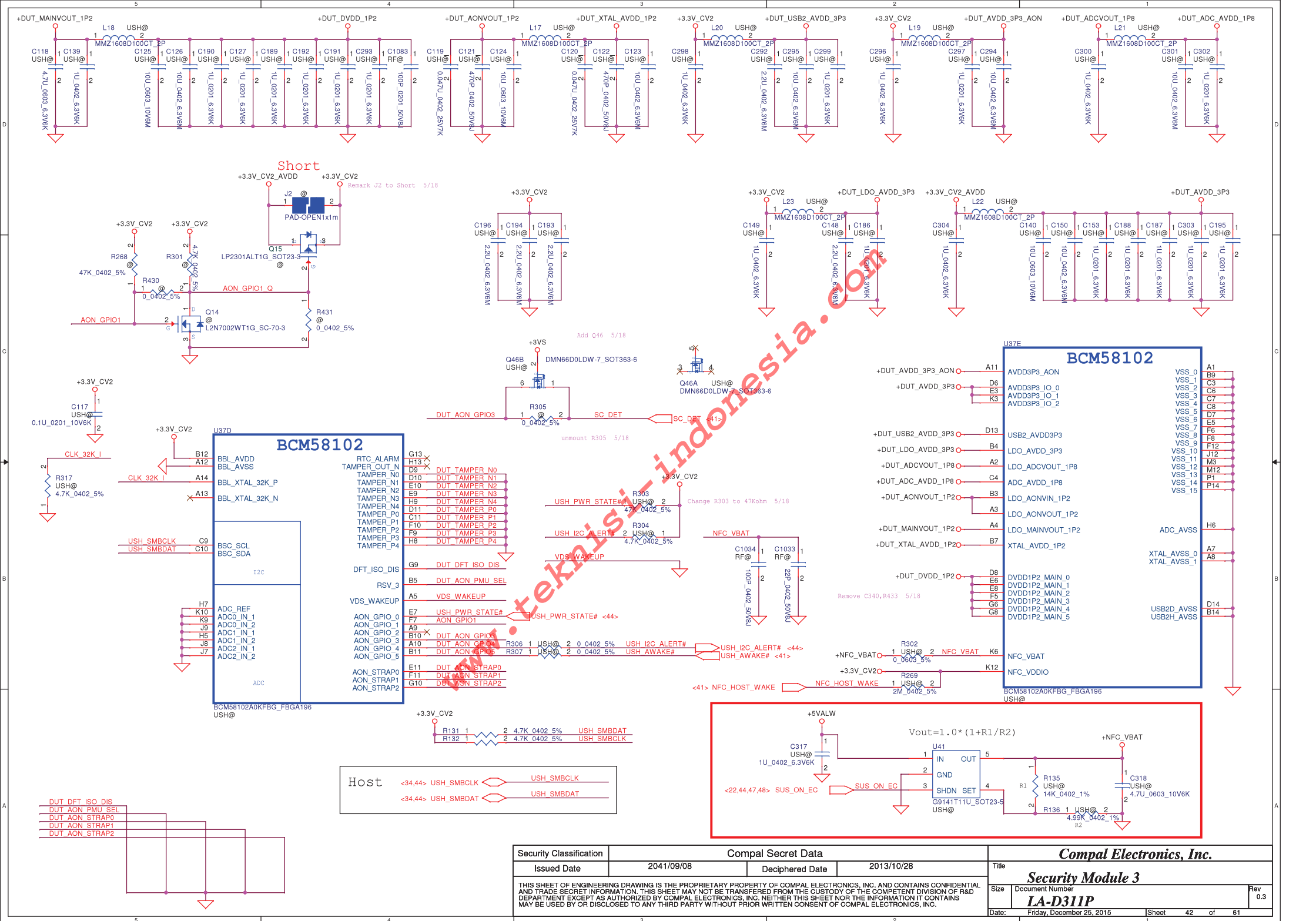
remove R276, R277 5/18



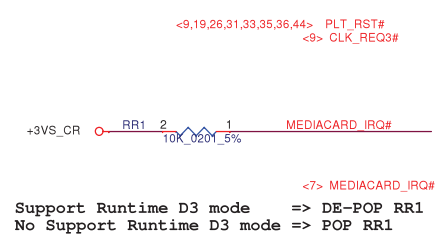
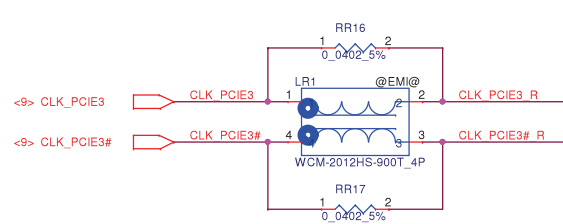
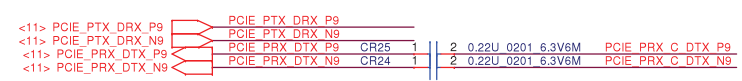
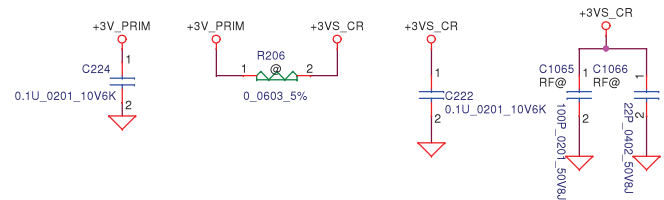
unmount C272 5/26



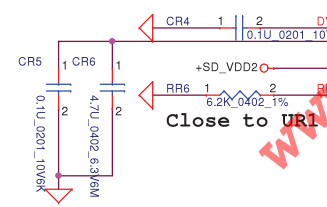
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		51			

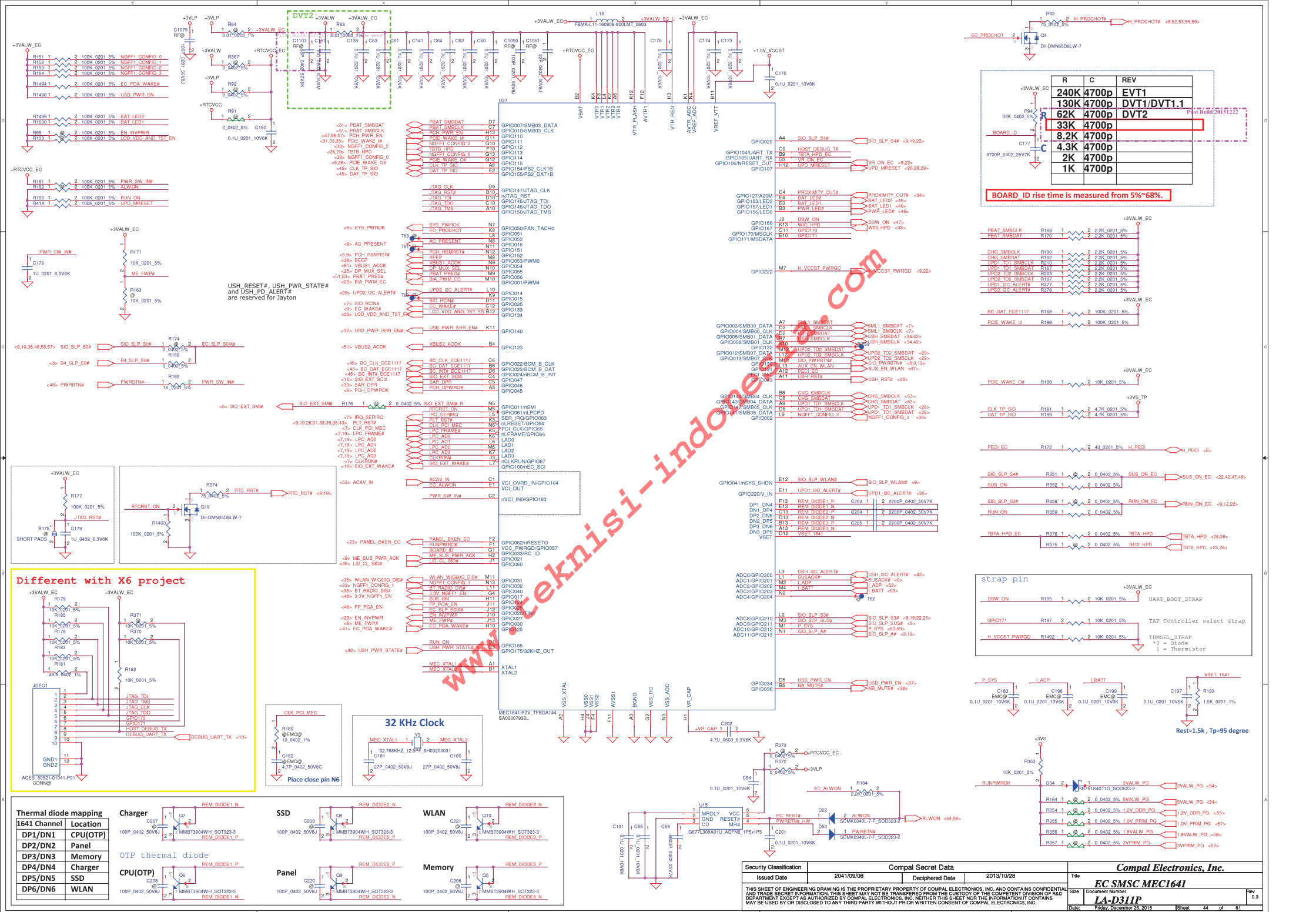


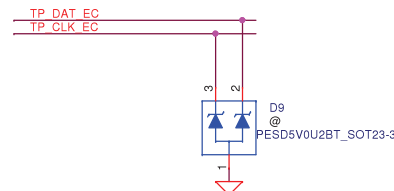
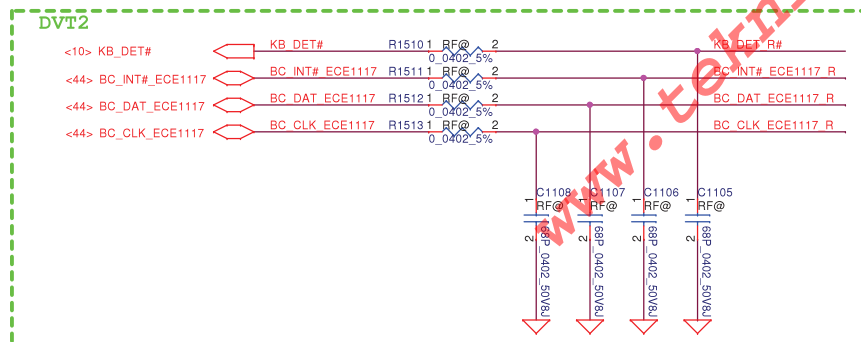
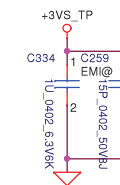
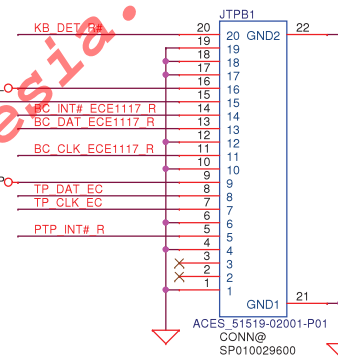
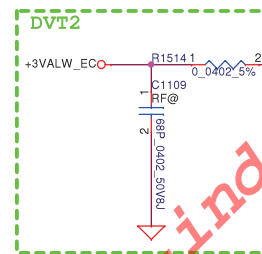
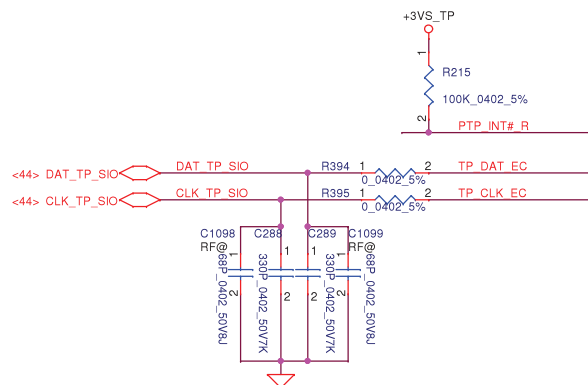
Card Reader



Support Runtime D3 mode => DE-POP RR1
No Support Runtime D3 mode => POP RR1





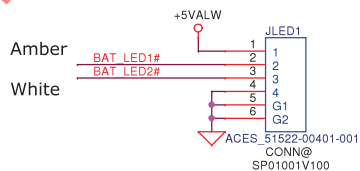


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The diagram illustrates the Standoff dataset components and their connections. It is divided into several sections:

- Top Row:** Components H23, H24, H25, H26, H39, H40, H36, H37, and H38. Each component is represented by a blue circle with a white dot in the center, connected to a red triangle (ground) via a red line. The connections are labeled with text like H_2P2X3P4N, H_2P2, H_2P2, H_2P2, H_1P2N, H_1P2X1P4N, H_2P0N, H_2P0N, and H_2P5.
- Bottom Row:** Components H31, H32, H34, H33, H35, H42, and H41. Each component is represented by a blue circle with a white dot in the center, connected to a red triangle (ground) via a red line. The connections are labeled with text like H_3P5, H_3P5, H_3P5, H_3P5, H_3P5, H_0P9N, and H_0P8N.
- Right Side:** Components FD1, FD2, FD3, and FD4. Each component is represented by a blue circle with a white dot in the center, connected to a red triangle (ground) via a red line. The connections are labeled with text like FIDUCIAL_C40M80.
- Center:** Components H27, H28, H29, and H30. Each component is represented by a blue circle with a white dot in the center, connected to a red triangle (ground) via a red line. The connections are labeled with text like ME@H_3P3, ME@H_3P3, ME@H_3P3, and ME@H_3P3.
- Bottom Center:** The word "Standoff" in a large, blue, serif font.

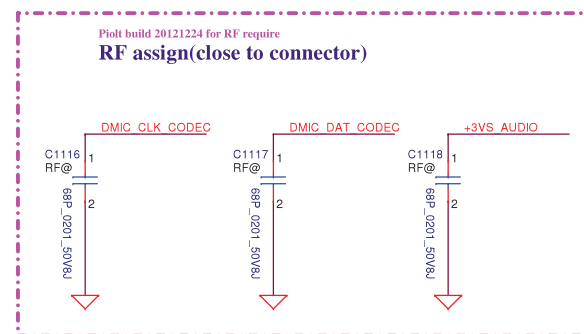
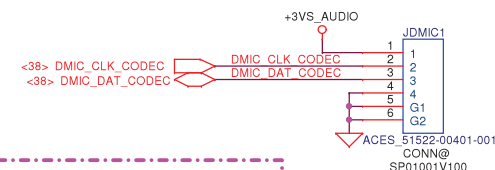
CLP1	CLP7	CLP13	CLP19	CLP25	CLP31	CLP37	CLP43
ECom5000700 EMIST_SUL-12A2M_1P CLP2	ECom5000700 EMIST_SUL-12A2M_1P CLP8	ECom5000700 EMIST_SUL-12A2M_1P CLP14	ECom5000700 EMIST_SUL-12A2M_1P CLP20	ECom5000700 EMIST_SUL-12A2M_1P CLP26	ECom5000700 EMIST_SUL-12A2M_1P CLP32	ECom5000700 EMIST_SUL-12A2M_1P CLP38	ECom5000700 EMIST_SUL-12A2M_1P CLP44
ECom5000700 EMIST_SUL-12A2M_1P CLP3	ECom5000700 EMIST_SUL-12A2M_1P CLP9	ECom5000700 EMIST_SUL-12A2M_1P CLP15	ECom5000700 EMIST_SUL-12A2M_1P CLP21	ECom5000700 EMIST_SUL-12A2M_1P CLP27	ECom5000700 EMIST_SUL-12A2M_1P CLP33	ECom5000700 EMIST_SUL-12A2M_1P CLP39	ECom5000700 EMIST_SUL-12A2M_1P CLP45
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ECom5000700 EMIST_SUL-12A2M_1P CLP6	ECom5000700 EMIST_SUL-12A2M_1P CLP12	ECom5000700 EMIST_SUL-12A2M_1P CLP18	ECom5000700 EMIST_SUL-12A2M_1P CLP24	ECom5000700 EMIST_SUL-12A2M_1P CLP30	ECom5000700 EMIST_SUL-12A2M_1P CLP36	ECom5000700 EMIST_SUL-12A2M_1P CLP42	ECom5000700 EMIST_SUL-12A2M_1P CLP48
ECom5000700 EMIST_SUL-12A2M_1P CLP1	ECom5000700 EMIST_SUL-12A2M_1P CLP7	ECom5000700 EMIST_SUL-12A2M_1P CLP13	ECom5000700 EMIST_SUL-12A2M_1P CLP19	ECom5000700 EMIST_SUL-12A2M_1P CLP25	ECom5000700 EMIST_SUL-12A2M_1P CLP31	ECom5000700 EMIST_SUL-12A2M_1P CLP37	ECom5000700 EMIST_SUL-12A2M_1P CLP43



Power Button + LED

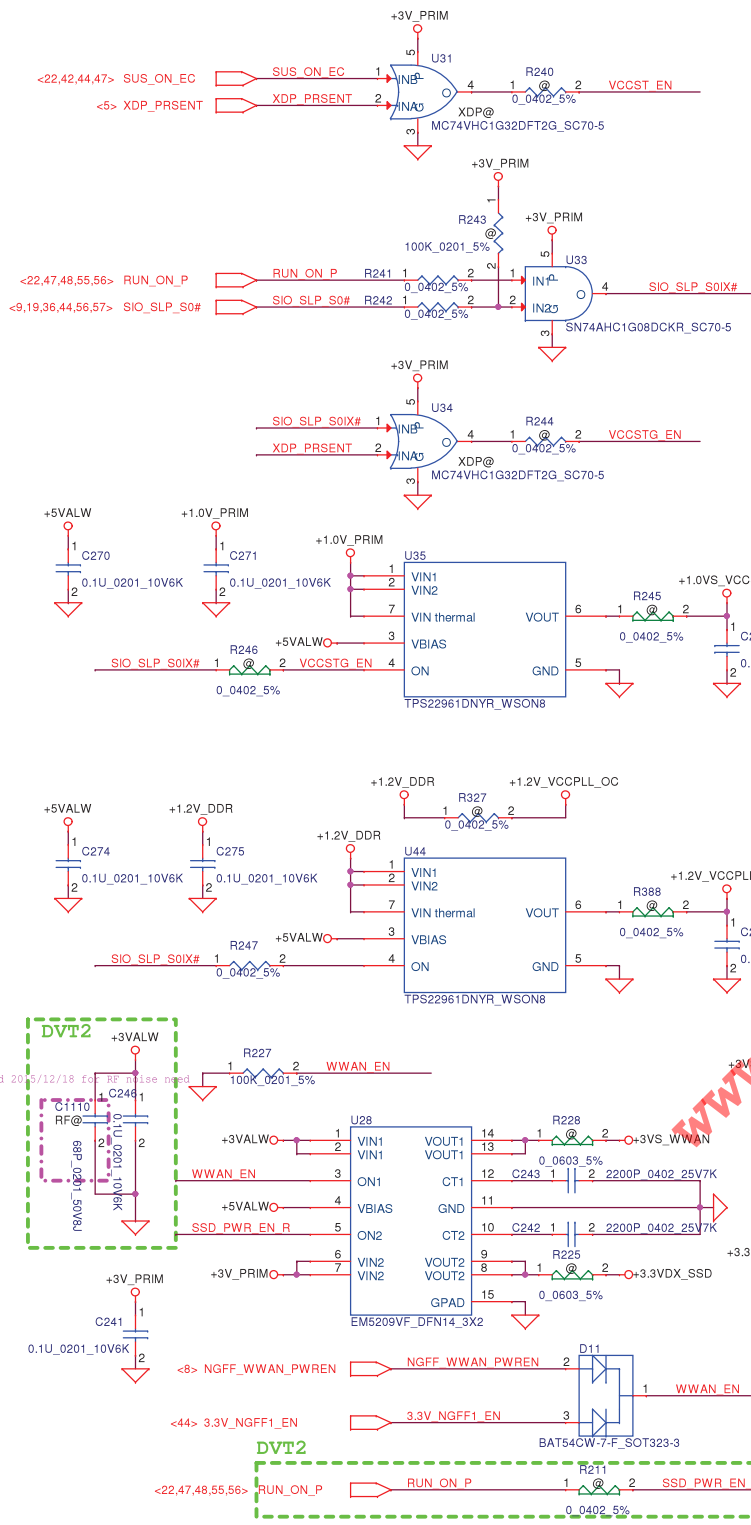
EC GPIO set to OD output

The diagram shows a schematic for a power button and LED. On the left, a component labeled 'TWAS1202AB0_SOT23-3' is shown with pins 1, 2, and 3. Pin 1 is labeled 'EM1@' and is connected to ground. Pin 2 is connected to 'PWR_LED#'. Pin 3 is connected to 'PWRBTN#'. A diode 'D49' is connected between pins 2 and 3. On the right, a component labeled 'LED1' (HT-F196BPS_WHYE) is shown with pins 1 and 2. Pin 1 is connected to 'PWR_LED#'. Pin 2 is connected to 'PWRBTN#'. A switch 'SW3' is connected between pins 1 and 2. A 3V3 supply is connected to pin 1. A 300_0402_5% resistor is connected between pin 2 and ground. The text 'EC GPIO set to OD output' is present.



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Close to PWR source



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DC/DC Interface 2

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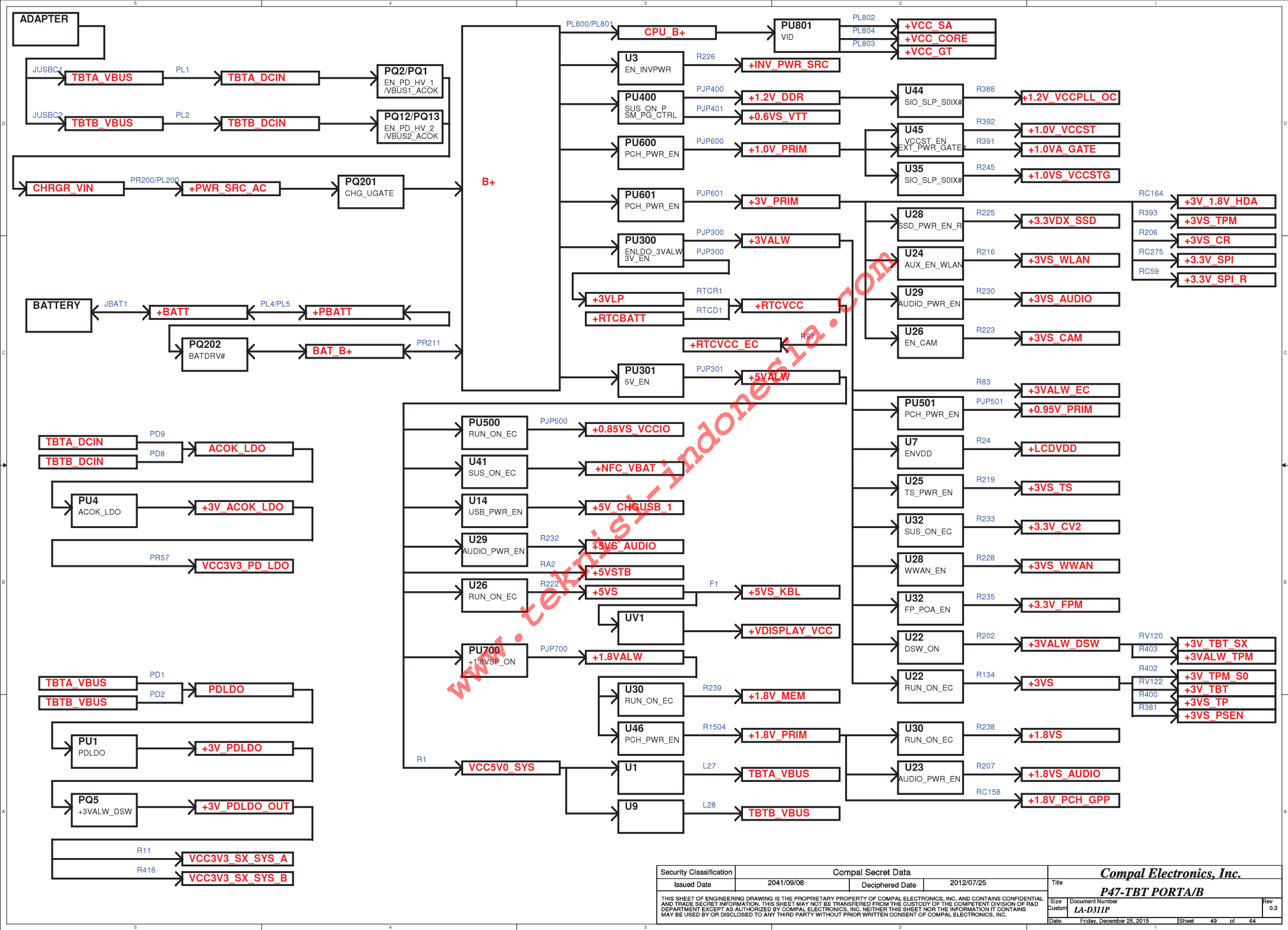
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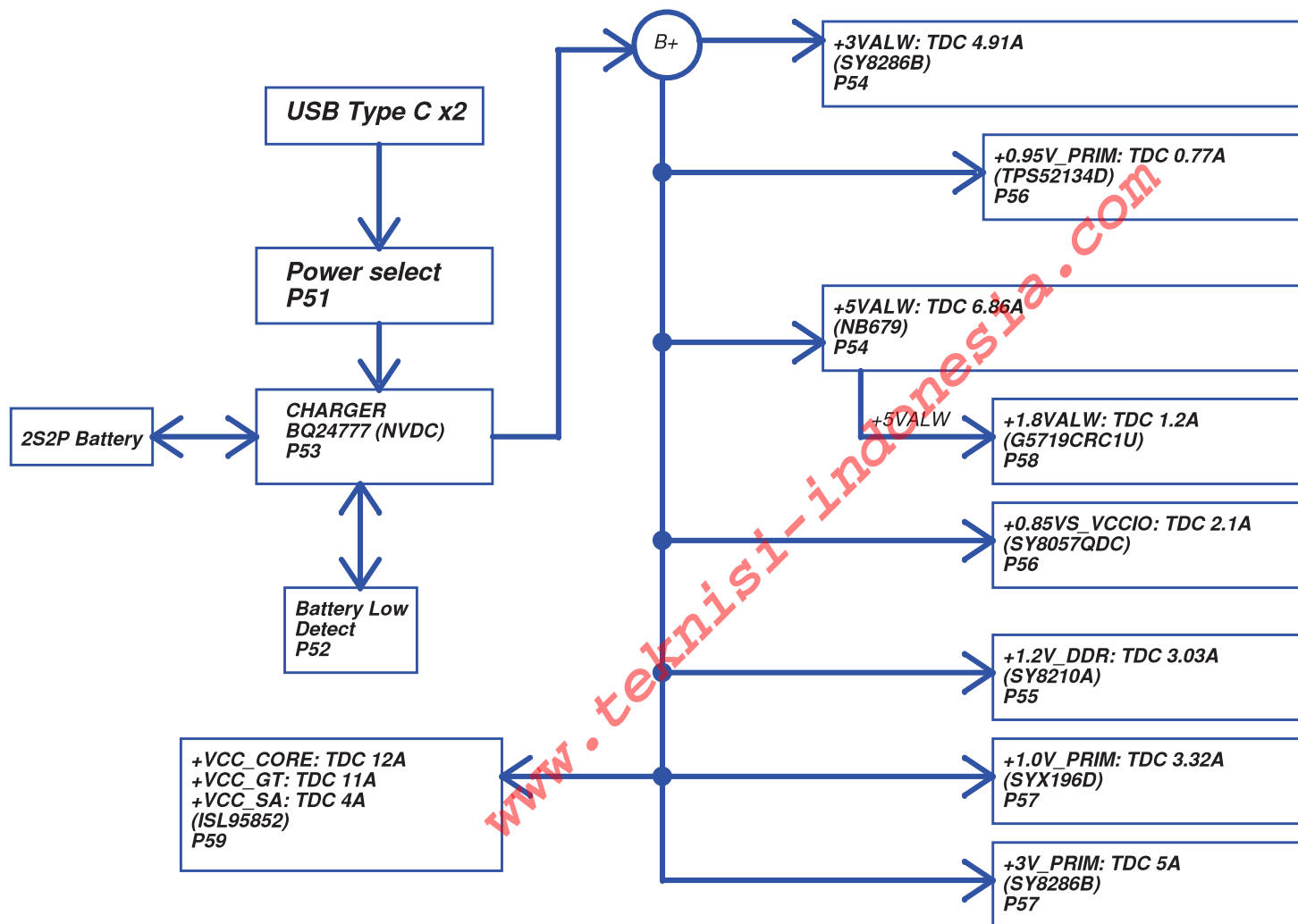
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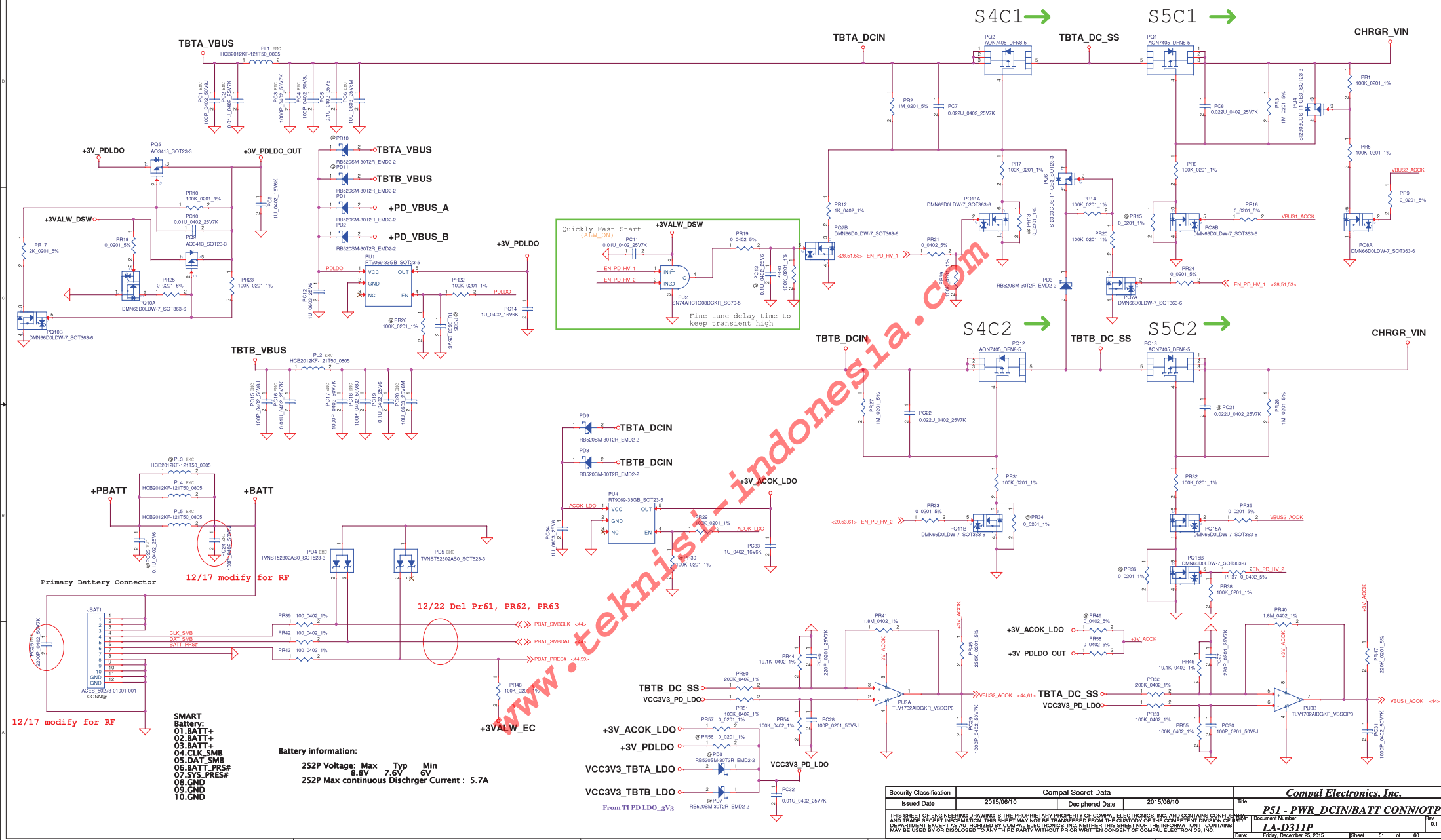
48

of

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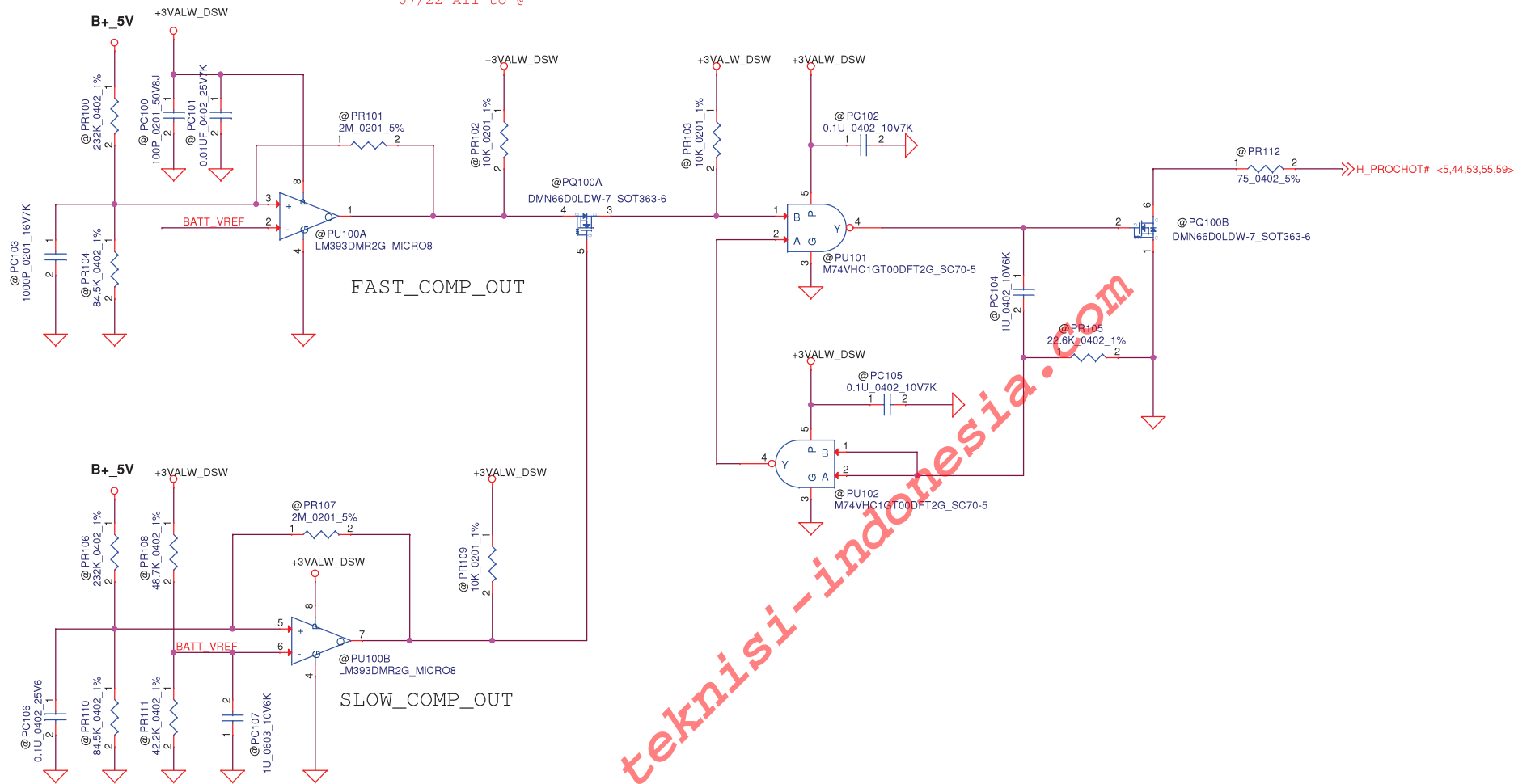




[illegible]

BATT low voltage detect

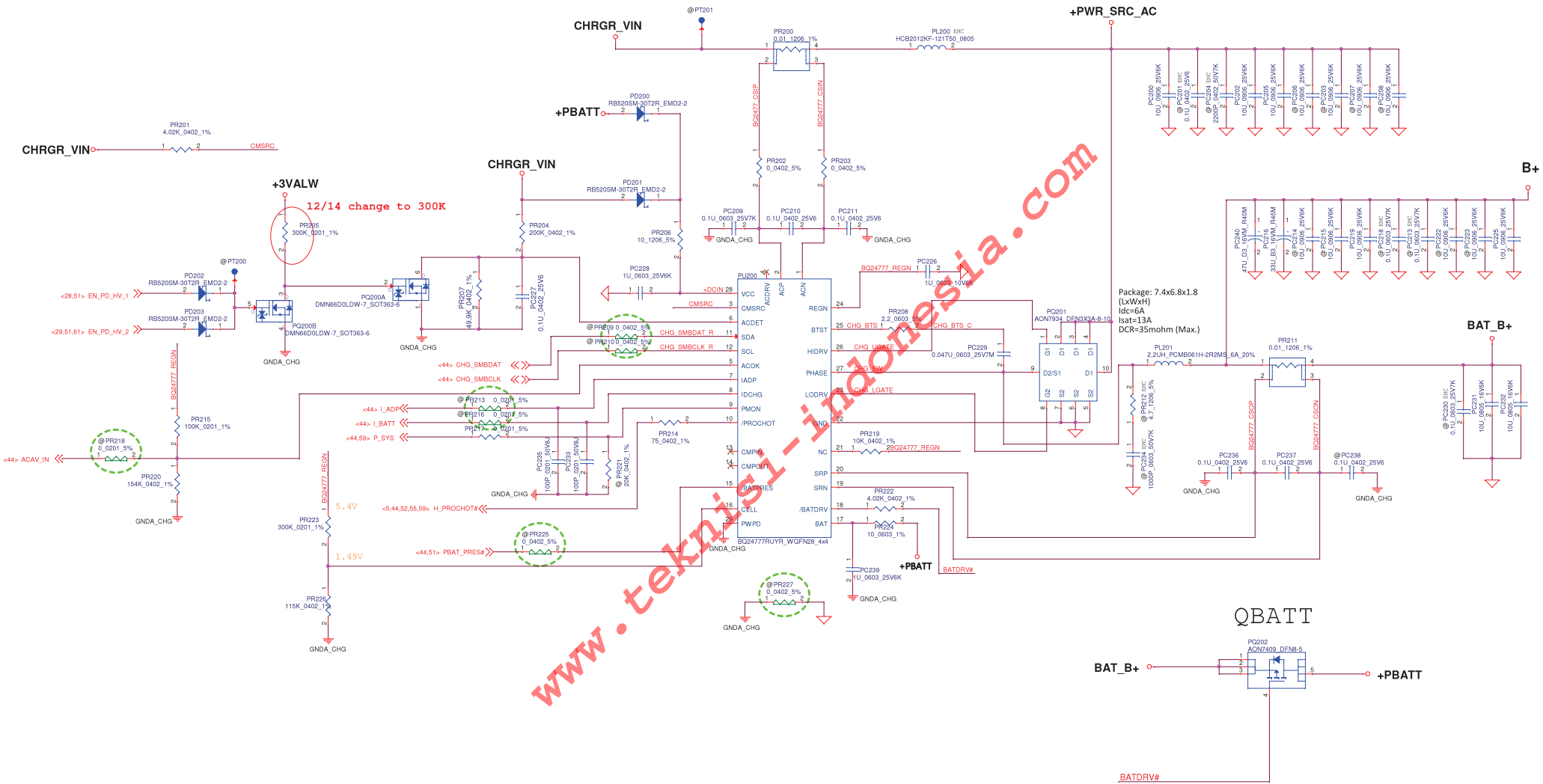
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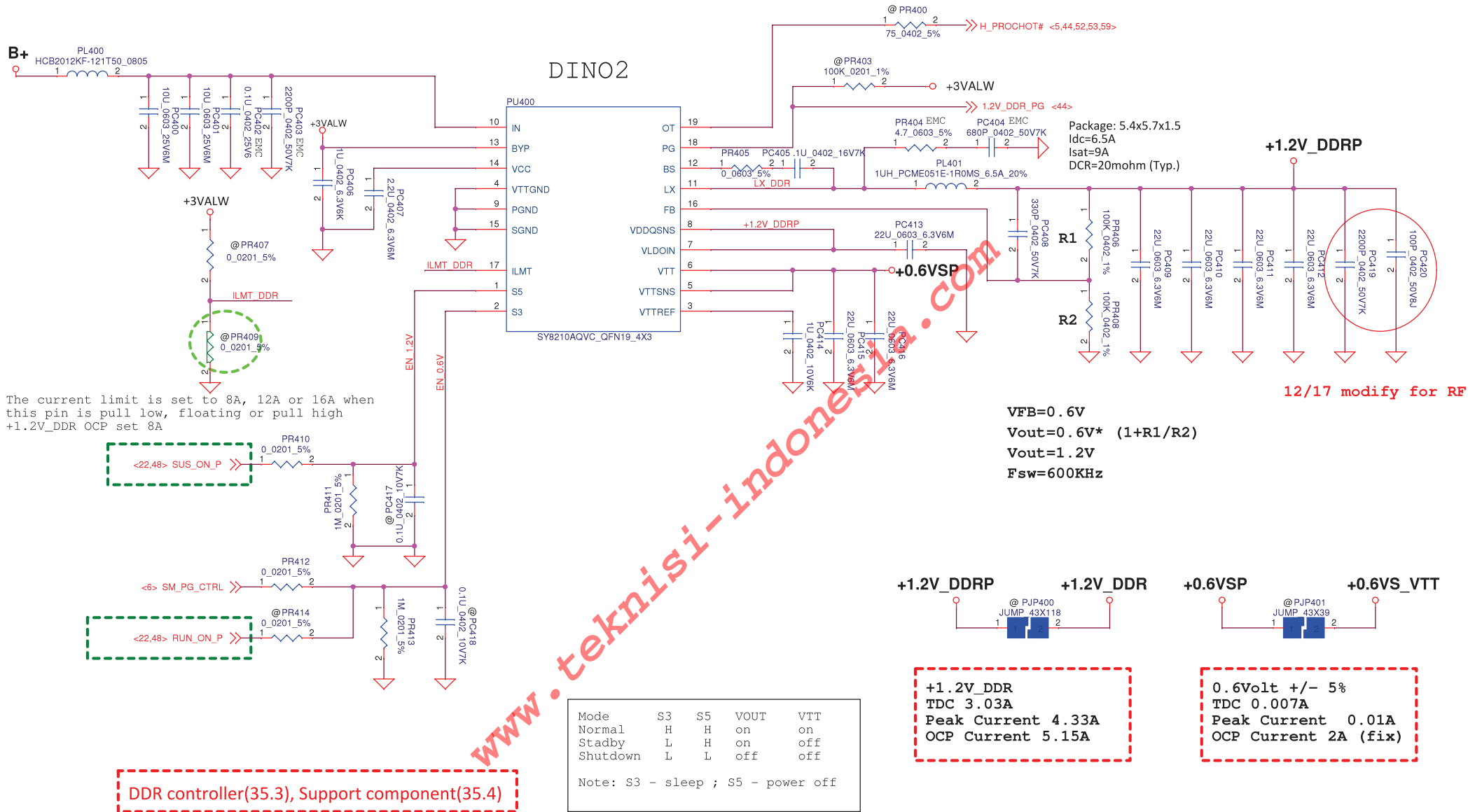
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Charger controller(40.1), Support component(40.2)

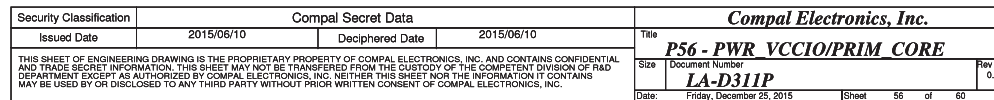


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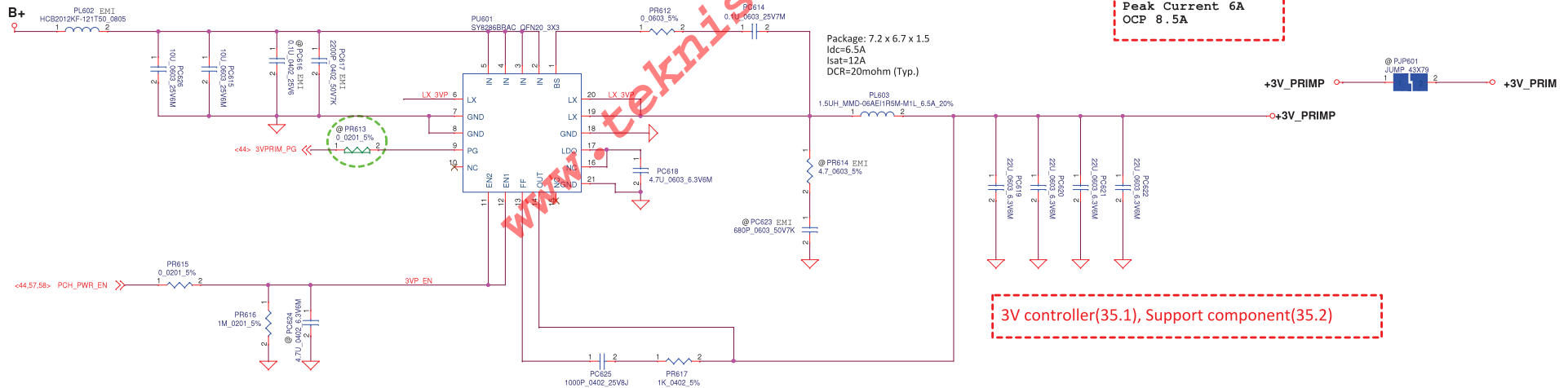
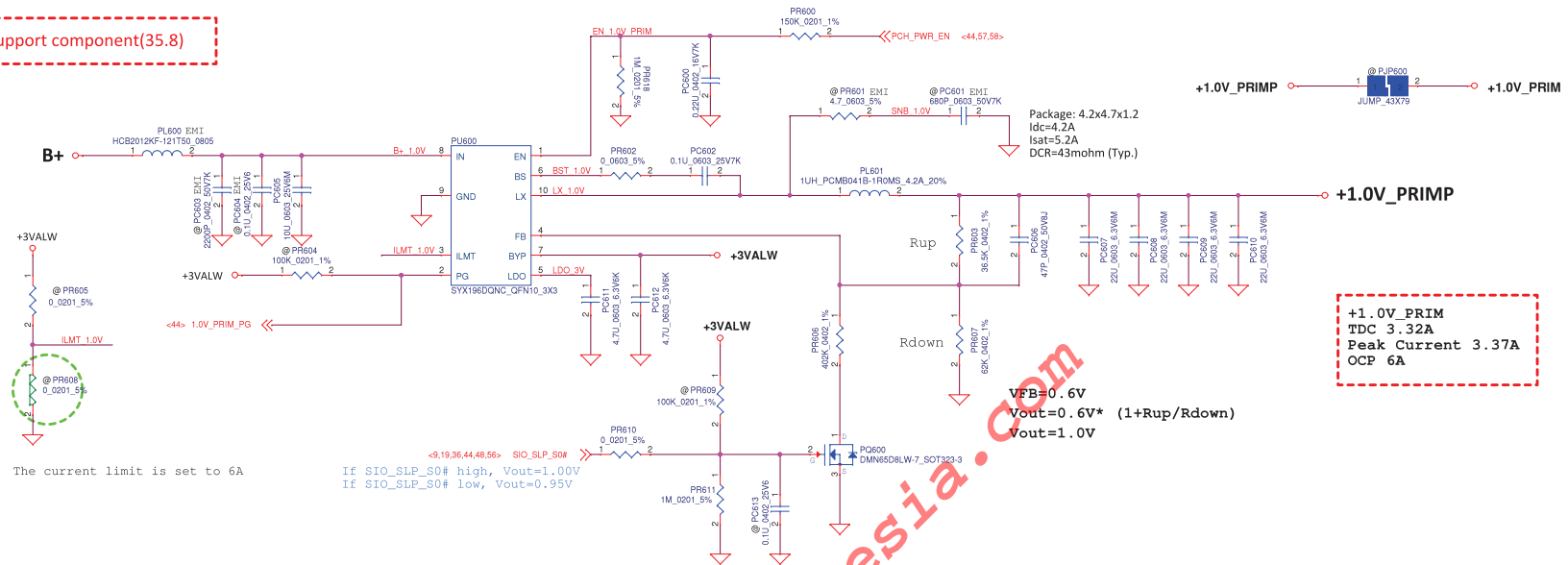


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The diagram shows the +3V_PRIM power plane. It features a 100k Ohm resistor network connecting the +3V_PRIM input to the VID0_VCCIO and VID1_VCCIO pins of the FR509 and FR510 components. The network consists of two 100k Ohm resistors in series, with the input voltage divided across them. The output voltage is labeled as VID0_VCCIO and VID1_VCCIO.

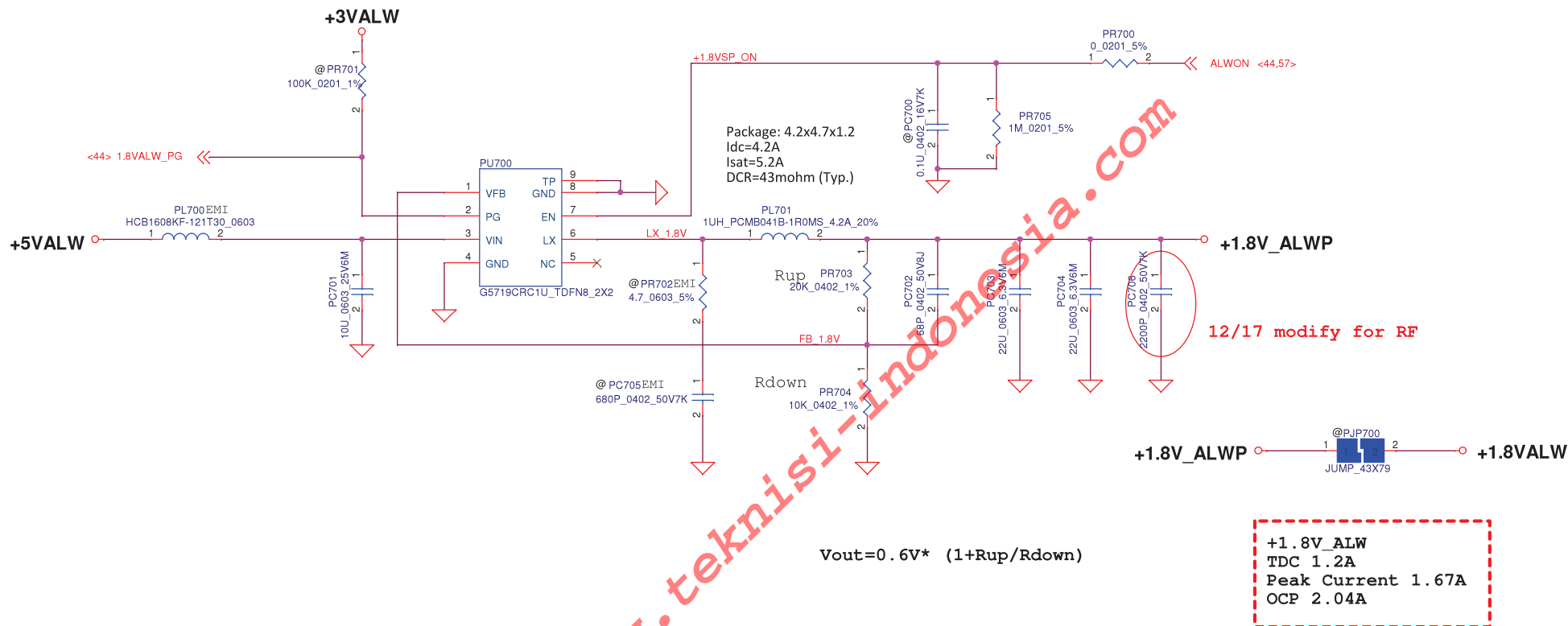


+1.0V_PRIM controller(35.7), Support component(35.8)



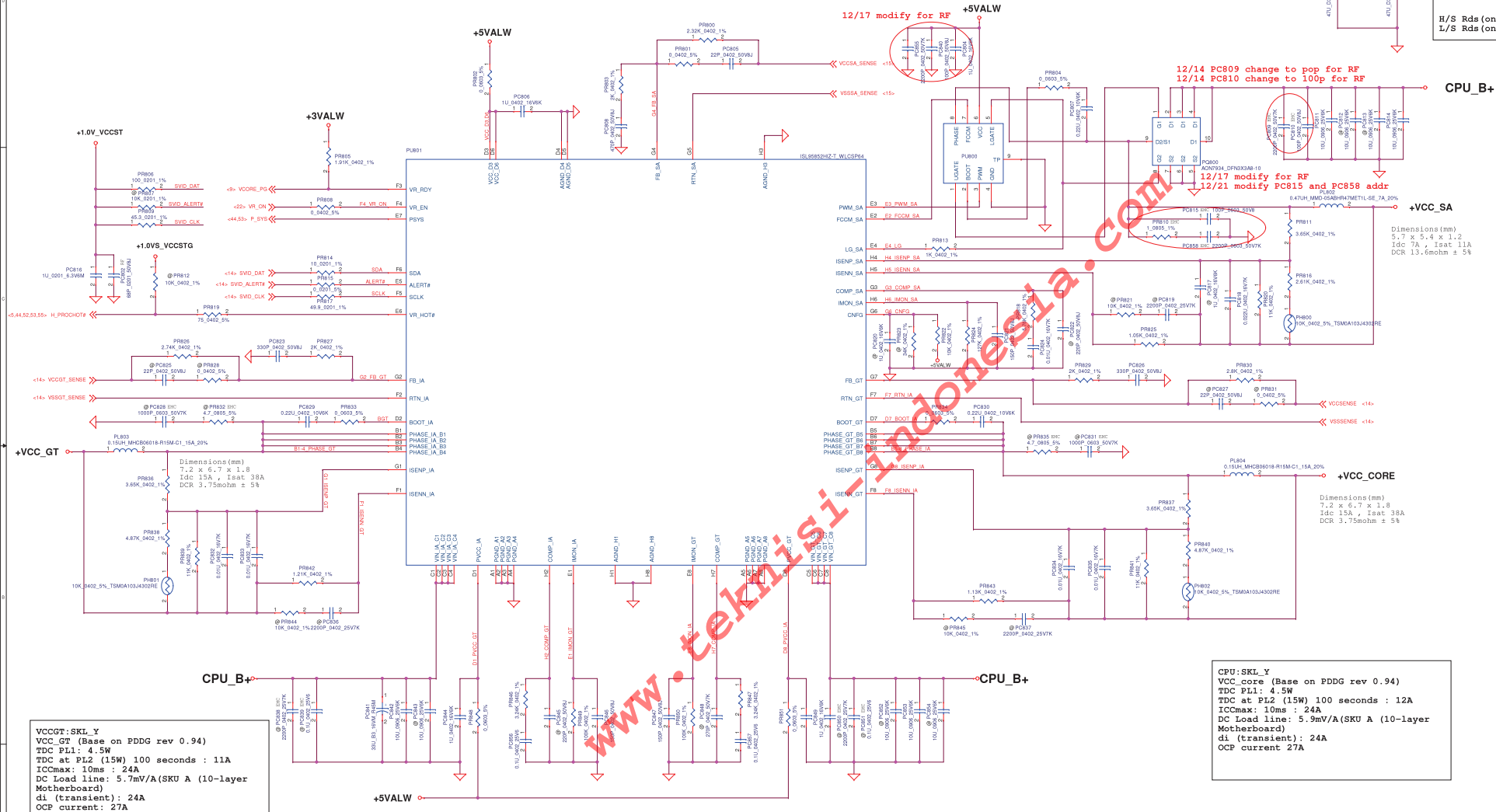
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1.8V controller(35.15), Support component(35.16)



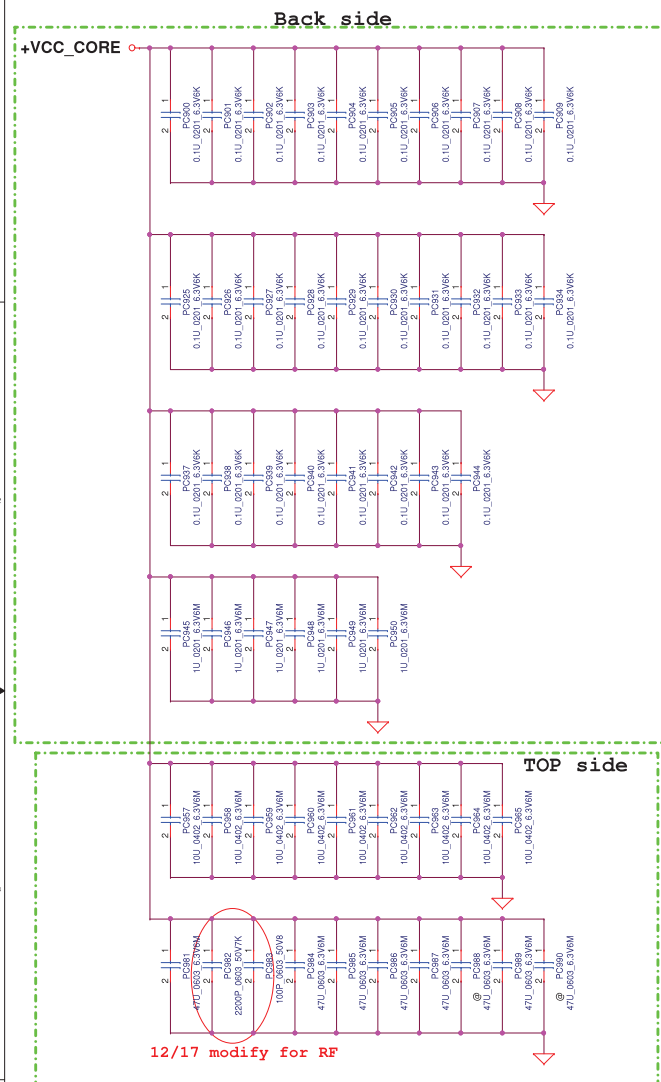
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VCORE/GT/SA controller(36.1), Drivers(36.2), Support component(36.3)



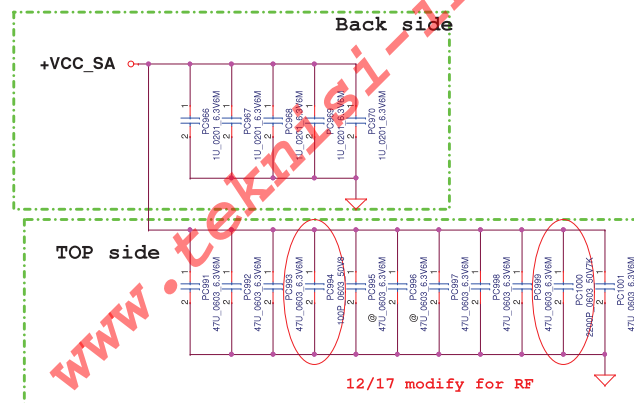
VCC_GT
0.1U_0201 * 15 pcs +1U_0201*6 pcs+1U_0402*4pcs+10U_0402*2pcs+47U_0603*13pcs

VCC_CORE
0.1U_0201 * 28 pcs +1U_0201*6 pcs+10U_0402*9pcs+47U_0603*10pcs

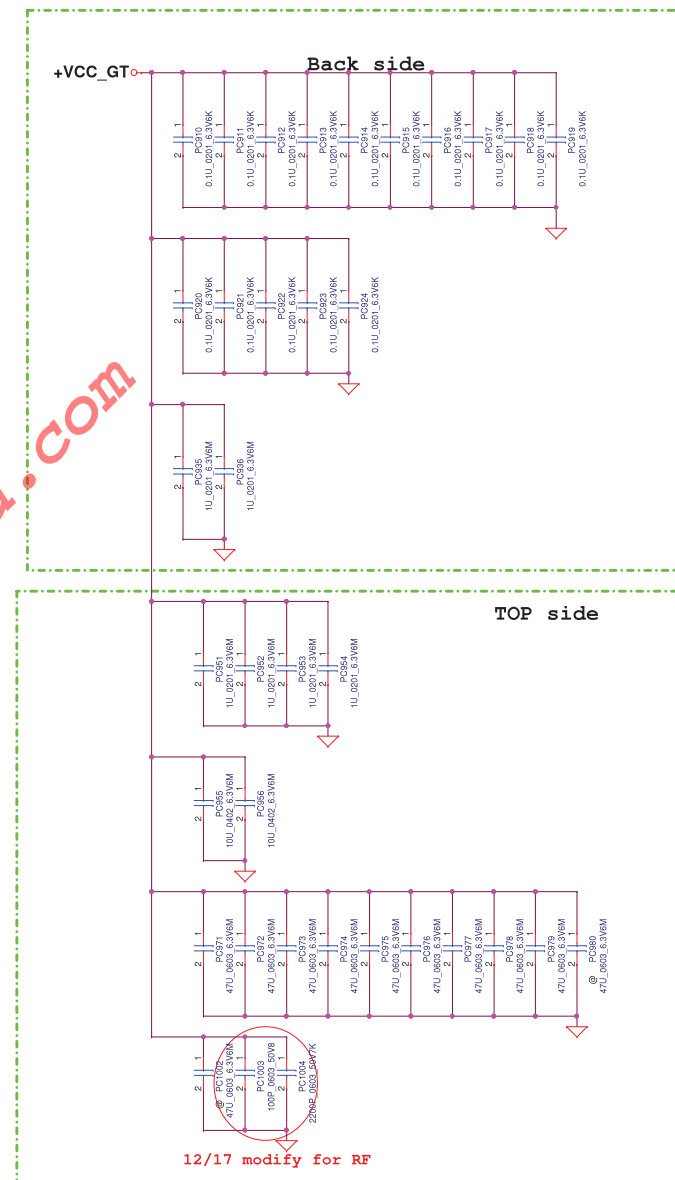


VCC_CORE output cap (36.4)

VCC_SA
1U_0201 * 5 pcs +47U_0603*11 pcs



VCC_SA output cap (36.6)



VCC_GT output cap (36.5)